INTERFACE™

MICROCOMPUTING FOR HOME AND SMALL BUSINESS VOL. 2, ISSUE 5, APRIL 1977 $1.50

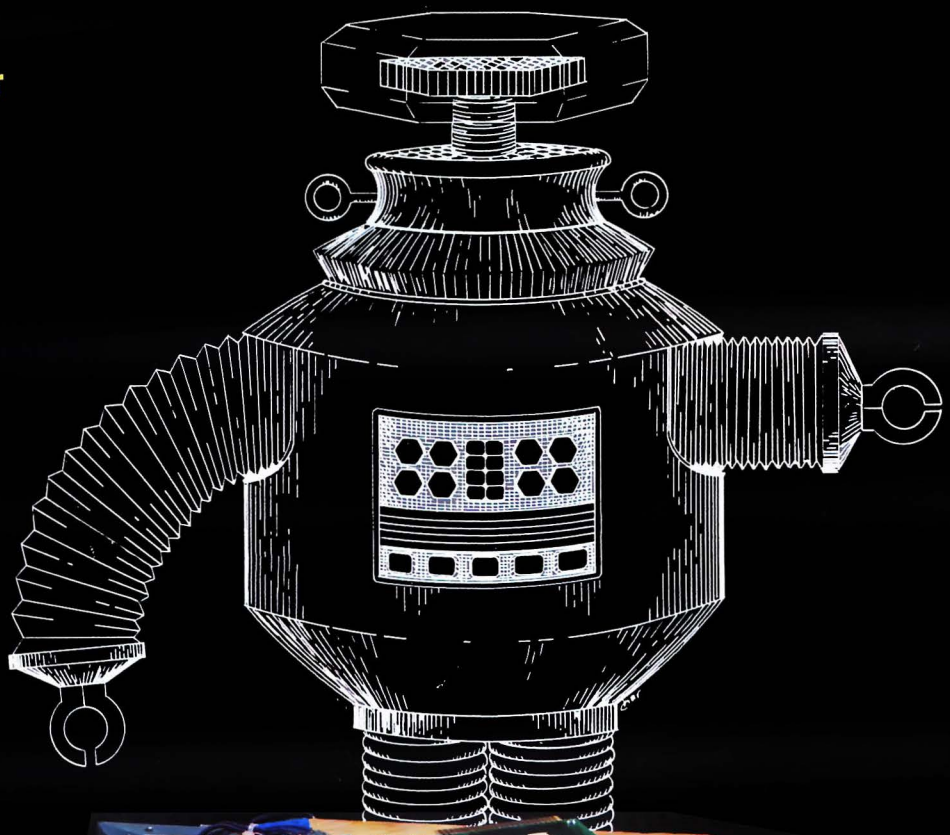
"Mike" — Computer Controlled Robot

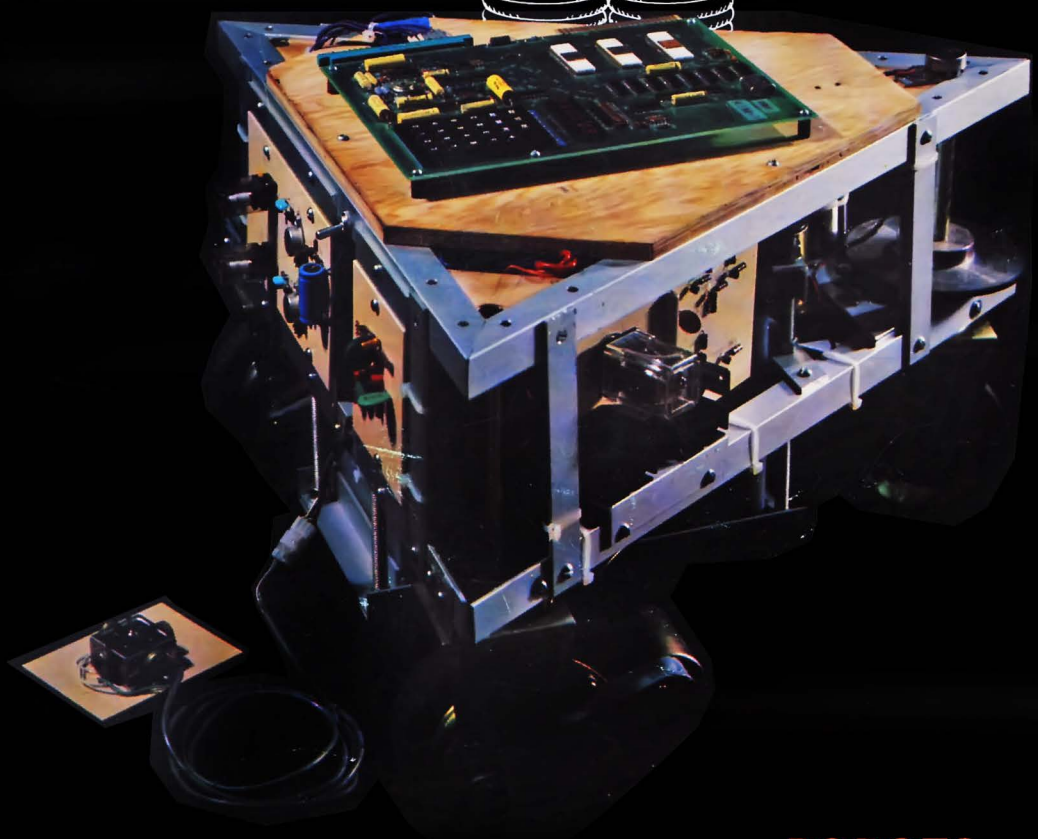
Robots as Household Pets

AROK

Building a Digital Group System

EXMON 6800 Extended Monitor System





ROBOTS — OUR FUTURE FRIENDS

Old Fashion VALUE in the U.S.A. Tradition

Our 6800 computer system represents the best value available today, with no sacrifice in performance.

I would like to explain why this is true. The most basic reason is that the 6800 is a simpler, more elegant machine. The 6800 architecture is memory oriented rather than bus oriented as are the older 8008, 8080 and Z-80 type processors. This is an important difference. It results in a computer that is far easier to program on the more basic machine language and assembly language levels. It also results in a far simpler bus structure. The 6800 uses the SS-50 bus which has only half the connections needed in the old S-100 (IMSAI/MITS) bus system. If you don't think this makes a difference, take a look at the mother boards used in both systems—compare them. The SS-50 system has wide, low impedance 0.1 lines with good heavy, easily replaced Molex connectors. The S-100 bus, on the other hand, has a very fine hair-like lines that must be small enough to pass between pins on a 100 contact edge connector. I'll give you one guess which is the most reliable and noise free. As for cost—well any of you who have purchased extra connectors for your S-100 machines know what kind of money this can run into. The 6800 is supplied with all mother board connectors. No extras, or options like memory, or connectors for the mother board are needed in our 6800 system.

The 6800 is not beautiful, but "Oh Boy" is it functional. That plain black box is strong and it has an annodized finish. This is the hardest, toughest finish you can put on aluminum. Most others use paint, or other less expensive finishes. The 6800 does not have a pretty front panel with lights and multicolor switches. This is because the lights and switches are not only expensive, and unnecessary, but also a great big pain to use. We don't crank up the 6800; we use an electric starter—a monitor ROM called Mikbug. He automatically does all the loading for you without any time wasting switch flopping. So in the 6800 system you don't buy something expensive (the console) that you will probably want to stop using as soon as you can get your hands on a PROM board and a good monitor.

That's another thing. Mikbug® is a standard Motorola part. It is used in many systems and supported by the Motorola software library in addition to our own extensive collection of programs. It is not an orphan like many monitor systems that are unique to the manufacturer using them and which can only run software provided by that manufacturer. Check the program articles in Byte, Interface and Kilobaud. You will find that almost all 6800 programs are written for systems using a Mikbug® monitor. Guess how useful these are if you have some off-brand monitor in your computer.

The 6800 will never win any beauty prizes. It is like the Model "T" and the DC-3 not pretty, but beautiful in function. It is simple, easy to use and maintain and does its job in the most reliable and economical way possible. What more could you want?

Mikbug ® is a registered trademark of Motorola Inc.

SWTPC 6800
Computer System
with serial interface and 4,096 words of memory $395.00

☐ Enclosed is $395 for my SwTPC Computer Kit ☐ Send Data

☐ or BAC_____ #_____

☐ or MC_____ Ex Date_____

NAME

ADDRESS

CITY STATE ZIP

Southwest Technical Products Corp., Box 32040, San Antonio, Texas 78284

CIRCLE INQUIRY NO. 41

Meet the most powerful μC system available for dedicated work. Yet it's only $595.*

Here's the muscle you've been telling us you wanted: a powerful Cromemco microcomputer in a style and price range ideal for your dedicated computer jobs—ideal for industrial, business, instrumentation and similar applications.

It's the new Cromemco Z-2 Computer System. Here's some of what you get in the Z-2 for only $595:

- The industry's fastest μP board (Cromemco's highly regarded 4 MHz, 250-nanosecond cycle time board).
- The power and convenience of the well-known Z-80 μP.
- A power supply you won't believe (+8V @ 30A, +18V and −18V @ 15A — ample power for additional peripherals such as floppy disk drives).
- A full-length *shielded* motherboard with 21 card slots.
- Power-on-jump circuitry to begin automatic program execution when power is turned on.
- S-100 bus.
- Standard rack-mount style construction.
- All-metal chassis and dust case.
- 110- or 220-volt operation.

DEDICATED APPLICATIONS

The new Z-2 is specifically designed as a powerful but economical dedicated computer for systems work. Notice that the front panel is entirely free of controls or switches of any kind. That makes the Z-2 virtually tamper-proof. No accidental program changes or surprise memory erasures.

FASTEST, MOST POWERFUL μC

Cromemco's microcomputers are the fastest and most powerful available. They use the Z-80 microprocessor which is widely regarded as the standard of the future. So you're in the technical fore with the Z-2.

BROAD SOFTWARE/PERIPHERALS SUPPORT

Since the Z-2 uses the Z-80, your present 8080 software can be used with the Z-2. Also, Cromemco offers broad software support including a monitor, assembler, and a BASIC interpreter.

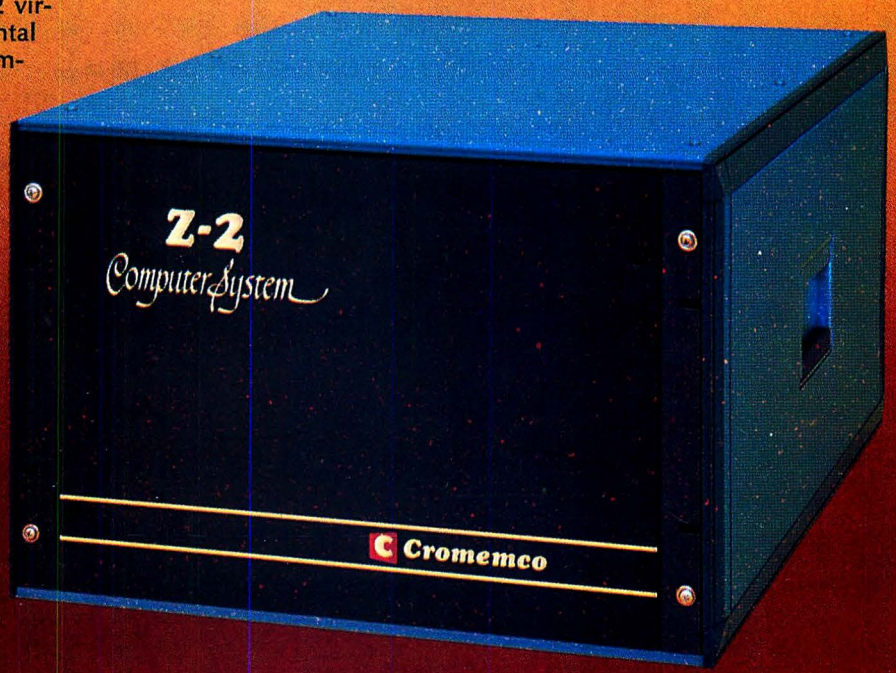
The Z-2 uses the S-100 bus which is supported by the peripherals of dozens of manufacturers. Naturally, all Cromemco peripherals such as our 7-channel A/D and D/A converter, our well-known BYTESAVER with its built-in PROM programmer, our color graphics interface, etc., will also plug into the S-100 bus.

LOW, LOW PRICE

You'll be impressed with the Z-2's low price, technical excellence and quality. So see it right away at your computer store—or order directly from the factory.

Z-2 COMPUTER SYSTEM KIT (MODEL Z-2K) (includes 4 MHz μP card, full-length 21-card-slot motherboard, power supply, one card socket and card-guide set, and front panel; for rack mounting) . . . . . $595.

Z-2 COMPUTER SYSTEM ASSEMBLED (MODEL Z-2W) (includes the above as well as all 21 sockets and card guides and a cooling fan; for rack mounting) . . . $995.



Shown with optional bench cabinet

*kit price

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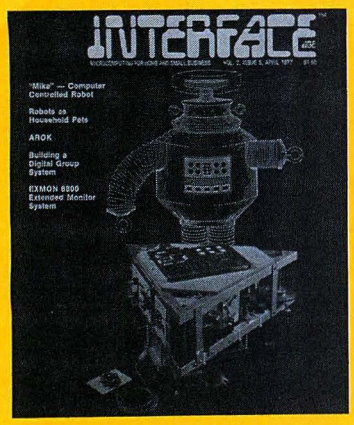

A triangular platform on wheels, a KIM-1 microcomputer, hours of labor and a supportive parent are the ingredients that built "Mike". Our thanks and praise go to John Loofbourrow, Tod's father, who supplied the cover photography, edited and typed the son's manuscript and supplied the permission for publication.

John and Tod are members of ACGNJ, Amateur Computer Group of New Jersey. The club will receive a $25.00 bonus over and above Tod's honorariun.

The "ghosted" figure was inspired by "Robot" from "Lost in Space", courtesy 20th Century Fox Television.

INTERFACE age™

MICROCOMPUTING FOR HOME AND THE SMALL BUSINESSMAN

FEATURES

PRODUCT REVIEW

HARDWARE FEATURES

SOFTWARE FEATURES

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Print Your Heart Out.

With help from the Digital Group, naturally.

Now, that small computer system you own or have been considering for personal or business use suddenly becomes a lot more usable—with the addition of a full-size *impact* printer from the Digital Group. A printer designed for small computers that need big output (like yours).

With the Digital Group printer, you can print your heart out...and it won't cost an arm and a leg. The Digital Group printer is available for less than $500. That's right—$500.

Just look at these specifications:

- Fast—120 characters per second
- 96 characters per line
- 12 characters per inch horizontal
- 6 lines per inch
- Makes up to 4 copies simultaneously
- Character set and pitch variable under software control—double width characters, etc.
- 5 x 7 character matrix
- Ribbon has built-in re-inkers for a life of 10,000,000 characters
- Paper can be either a standard 8½-inch roll, fanfold or cut page
- Interfaces to 8-bit parallel ports

There are lots of capabilities and outstanding features of the Digital Group printer...and (as always) the best news is our price. Kit prices start as low as $495 for the printer and interface card. It simply can't be beat.

Find out all the facts about the Digital Group printer now. Just fill in the coupon below or give us a call for the details. We think you'll find a place for our printer in your system ...and in your heart.

the digital group

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Quick. I want to print my heart out.
Send me all the details on your full-size impact printer.

Name _____

Address _____

City/State/Zip _____

Please print.

INTERFACIAL

We continue this month with our introductions of the people who "procreate" the monthly editions of INTERFACE AGE. In previous issues you have met the production staff, home office editor, columnist, layout and art personnel. That is still only a part of the team. In coming issues we want to present our hard-working field team.

This month the column belongs to one man—the keystone of the arch: Robert S. Jones, Publisher and Editor-in-Chief, sire and *paterfamilias* of the magazine.

Robert S. Jones has eleven years' experience in electronics and semiconductor sales and marketing. This background has laid a firm base for Mr. Jones' entry into the publishing world.

Educated in Business Administration with a Marketing Major, Mr. Jones served for several years in microcomputer sales for INTEL and National Semiconductor, where he became aware of the need for information to reach the rapidly growing population of microcomputer users. This awareness took form in the founding of INTERFACE AGE.

* * *

This month's theme is ROBOTICS—the most challenging and fascinating field of endeavor for microprocessor users.

Admit it: as you were putting your kit together, did you not entertain dreams—if only momentarily—that your device would develop into something more . . .? For some people that dream has come true.

It came true for 15-year-old Tod Loofborrourrow and he tells us about it in his own words in MIKE—A COMPUTER-CONTROLLED ROBOT.

Not to be outdone as author and builder Tod's 7-year-old brother, Nathan offers his introductory efforts in the field of electronics in L.E.D. FLASHER.

The United States Robotics Society proposes a whimsical application in ROBOTS AS HOUSEHOLD PETS.

In a Chicago suburb a robot takes the family pet for a walk. No joke! The pictures that accompany AROK are for real.

That is only the beginning ; CMOS technology may give way to more refined methods. At that time designers of THE REMOTOID/ANDROID PROJECT may not be engaging in flights of s.f. fantasies, rather informing our readers of applications for the miniaturized components of this daughter generation of small computers.

Roger Edelson's corner brings us back from the whimsical to the concrete. In BUILDING A DIGITAL GROUP SYSTEM, Donald Southwick shares his successes and frustrations from kit delivery to completed system. A distinguished scientist, Kris Rallapalli reports on a PROGRAMMABLE BIT RATE GENERATOR.

Robert Stevens again supplies our readers with software features and fames. Lorin Mohler solves some COS problems in A PROPOSED CASSETTE DATE STORAGE FORMAT STANDARD. Is EXMON your interest? Michael Burton extends MIKBUG™'s monitor formware with upgraded commands.

In keeping with the futuristic theme of the issue, the space game, SHOOTING STARS is presented.

INTERFACE AGE
MAGAZINE

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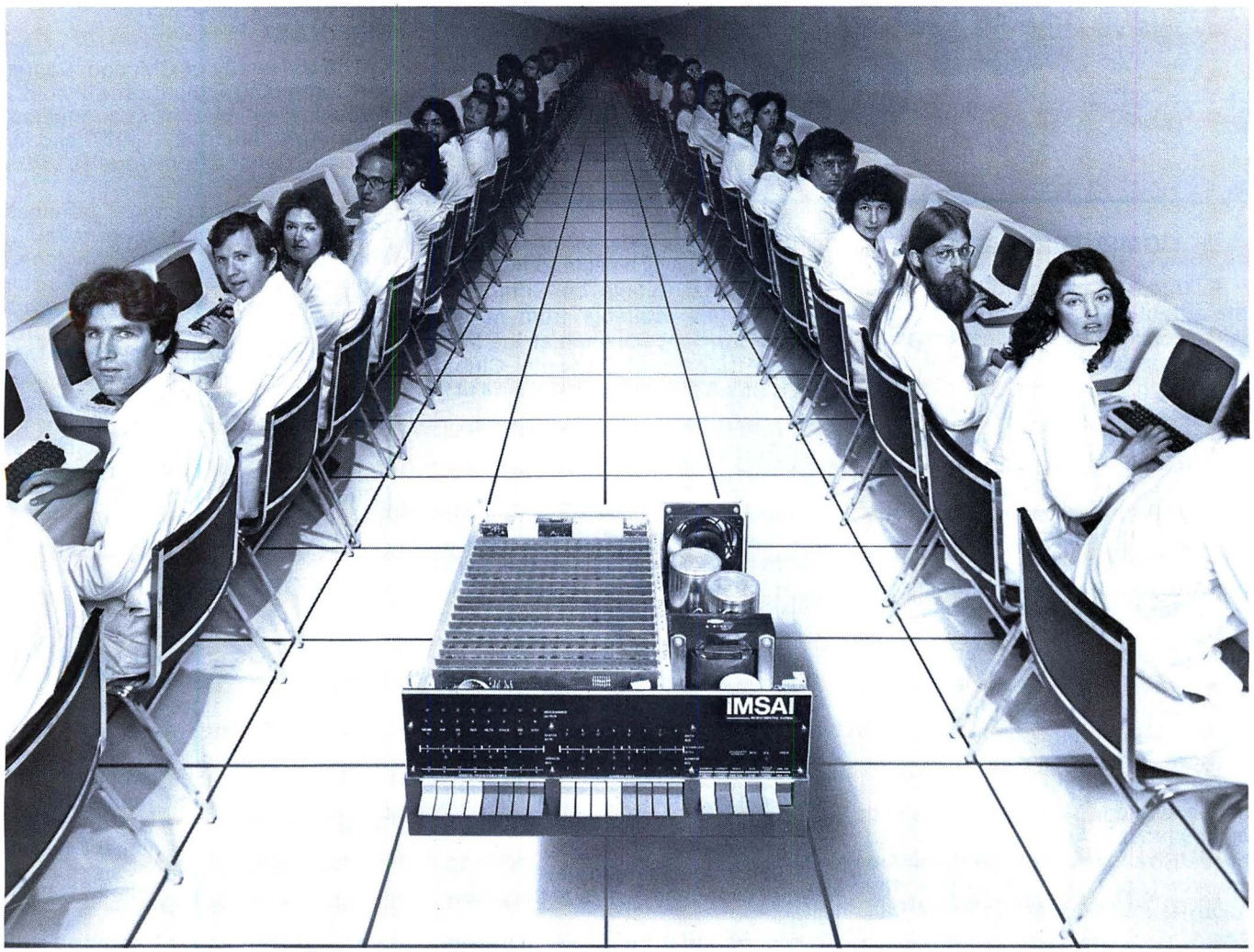

IMSAI Introduces the Megabyte Micro.™

The Megabyte Memory

Until today, the largest memory you could fit and address in a single microcomputer CPU was 65K.

Now, IMSAI presents an incredible memory system for micros 16 times more powerful than yesterday's best.

Imagine, a full megabyte of power from sixteen 65K RAM boards.

And, to control all this, the IMSAI Intelligent Memory Manager (IMM), the super control board.

You can write protect blocks throughout the full megabyte. Or, map in 16K blocks.

Plus, preset 16 mapping configurations with protect for high speed transfer or rapid change.

All interrupts are fully vectored, and there's an interrupt if an attempt is made to write into protected memory.

There's even a real "time of day" clock.

65K, 32K and 16K RAM Boards

Until today, the most memory you could plug into a single slot was 16K.

Now, IMSAI presents memory boards in astonishing multiples of sixteen: 65K, 32K and 16K low power, dynamic RAM Boards. They can be used in any S-100 bus computer individually or in combination to form conventional systems up to 65K bytes.

Every board is fast. With "hidden refresh" and *no* "wait state."

The Complete Megabyte Microcomputer System

The IMSAI Megabyte Micro™ is only part of the story. The full system can include dual floppy disks, terminals, plotters, printers and tape cassettes.

IMSAI also offers the finest high level and peripheral software available. Paper tape and Tape Cassette I/O and super Disk Operating Systems. Plus, BASIC and Disk BASIC with more high level languages coming.

Until today, the microcomputer's potential was just something you talked about.

Now, you can put it to work. Powerfully.

GENTLEMEN: IA

I'm power hungry!

- ☐ Send 65K RAM Board Kit $2599 ☐ Assembled $3899
- ☐ Send 32K RAM Board Kit $749 ☐ Assembled $1099
- ☐ Send 16K RAM Board Kit $449 ☐ Assembled $679
- ☐ Send IMM ROM Control Kit $299 ☐ Assembled $399
- ☐ Send IMM EROM Control Kit $499 ☐ Assembled $699
- ☐ Send full catalog $1.00

Check/MO enclosed. Amt. $ _____

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UPdate

COMPUTERFEST '77

A large flea market will be among the attractions at Computerfest '77, the second annual Midwest Regional Computer Conference for hobbyist computing.

Sponsored by the Midwest Affiliation of Computer Clubs, an organization of amateur clubs in ten neighboring states and Canada, the convention will open on June 10 at the Bond Court Hotel in Cleveland.

Computerfest '77 will be a complete convention with workshops, manufacturers' exhibits, a flea market, seminars, and technical sessions open to all attendees.

The flea market is an important part of any personal computing show. Hobby computing, while getting cheaper and easier every day, still breed bargain hunters who delight in the buying, selling, and trading of equipment. And there seems to be many ready sources of used and surplus gear. A major part of the hobby is interconnecting these bargains.

MACC is a volunteer, non-profit organization. The ticket price remains at two dollars for all activities, including the seminars. This nominal admission charge is ample to cover the expenses incurred.

Since the majority of attendees including some of the exhibitors themselves want to hear ninety percent of the seminars, this is clearly impossible with overlapping and conflicting schedules. The solution is to hold only one seminar at a time. The talks will be televised concurrently in smaller rooms. This arrangement will create a more relaxed atmosphere, and will allow everyone to hear the speakers.

The second weekend in June was chosen because it is the time most schools are letting out and before anyone really goes on vacation. Computerfest '77 wants to attract as many high school and college students as it can.

Computerfest '77 will take place the weekend after the National Computer Convention. Computerfest '77's organizers are chartering a jet to Dallas and all will be able to fly down.

Additional details on Computerfest '77 are available from MACC President Gary Coleman at the Midwest Affiliation of Computer Clubs, P.O. Box 83, Cleveland, Ohio 44141.

SYMPOSIUM ON COMPUTER APPLICATION IN MEDICAL CARE

Papers describing all aspects of the computer's application to medical needs are requested for the Symposium on Computer Application in Medical Care, according to General Chairman Abund O. Wist and Technical Program Chairman F. Helmuth Orthner. Scheduled for October 3-5, 1977, in Washington, D.C., the symposium is co-sponsored by the Medical College of Virginia, The George Washington University Medical Center, Northern Virginia Section of IEEE, and the IEEE Computer Society.

Topics considered relevant to the symposium theme include the following:

monitoring the critically ill patient
processing EKGs and EEGs
on-line data acquisition
clinical laboratory systems
automatic health testing
medical decision-making
consultation systems
diagnostic scanners
advances in health care technology
hospital information systems
information systems for ambulatory care.

Prospective authors are asked to submit four (4) copies of an abstract outlining their 20-minute presentation by *April 25, 1977*. The abstract should clearly state (1) the purpose of the work, (2) its potential usefulness for medical care, and (3) what specific results have been obtained.

Authors may submit additional supporting material (for review purposes only) at their discretion. All material should be sent to Dr. F. Helmuth Orthner, Department of Clinical Engineering, School of Medicine and Health Sciences, The George Washington University, 2300 K Street, N.W., Washington, D.C. 20037.

Authors will be notified before *May 16, 1977*, and those whose papers are accepted will receive an author's kit. All papers will be published in the symposium proceedings.

MINICOMPUTERS, A THREE-DAY INTENSIVE SEMINAR

The University of Chicago, Center for Continuing Education will hold a three-day seminar in Los Angeles, from April 25 to 27, 1977 and in Toronto, Canada from June 13 to 15, 1977.

This specialized seminar examines the uses, economics, programming, and implementation of minicomputers. Subjects covered will be Minicomputer Architecture, Peripheral Equipment, Software, Microprogramming, Microprocessors, Distributed Processing, Communications, AOS's, Intelligent Terminals and Mini-base Business Systems.

For information and registration to University of Chicago, Center for Continuing Education, 1307 East 60th Street, Chicago, Ill. 60637, or call 212 953-7266.

CALL FOR PAPERS

Authors are invited to submit original papers on novel and recent developments in the field of Computer Science and Engineering education for a tutorial and workshop to be held in Williamsburg, Virginia, June 7 and 8, 1977. The program will emphasize, but not be limited to the following topics:

- The "core" of Computer Science and Engineering
- The Technical profile of a CSE graduate
- The integration of hardware and software courses
- Articulation between Junior Colleges and four-year curricula
- Laboratories, project manual and course development materials

Dr. Richard Merwin, distinguished educator and pioneer of the computer field will keynote the workshop. In addition, invited panels will critically evaluate the text of the new CSE Model Curricula proposed by the IEEE Computer Society Education Committee.

Potential authors in the U.S. and abroad are encouraged to submit three copies of their papers to: Professor Oscar N. Garcia, Program Chairman, Dept. of Electrical and Electronics Systems, University of South Florida, Tampa, FL 33620, (Phone: 813-974-2948).

Papers should be limited to 15 double-spaced typewritten pages, and should be received before April 1, 1977. Acceptance of the papers will be acknowledged by April 15, 1977. At that time or before the authors will receive instructions on the

Subsystem "B" makes the computer you already have work almost as well as a new Sol-20.

Add it now, and for a limited time we'll throw in a new module with 2048 bytes of preprogrammed PROM or ROM and 1024 bytes of RAM memory free!

Processor Technology's Subsystem "B" puts together the major system elements you need to get your Altair or IMSAI up and running.

You get both RAM and PROM memory, parallel, serial, cassette and video display interfaces, and software. Software includes a bootstrap loader program so you can load any Processor Technology CUTS ("Byte/Kansas City") 1200 BAUD cassette tapes. Standardized subroutines in ROM, similar to those in a Sol personality module, are used by many Processor Technology software packages to improve program efficiency. You'll find you rarely need to touch your front panel switches. With our Subsystem "B" you are up and running as soon as you turn on the power.

Three subsystems are available, depending on your memory requirements. Each Subsystem "B" includes five S-100 bus compatible modules as listed below. Each is dependent upon our new GPM module (GPM = General Purpose Memory) which provides 1024 bytes of low power static RAM and 2048 bytes of preprogrammed ROM or EPROM as well as space for up to 8192 bytes more of ROM or 2708 type EPROM. The GPM module accepts the new ROM version of our well known ALS-8 Editor/Assembler software package.

With Subsystem "B" you have guaranteed compatibility with all Processor Technology software and hardware products.

Subsystem Model	B70	B110	B190
Total memory provided (bytes)	7168	11264	19456
Display I/O	VDM-1	VDM-1	VDM-1
Parallel, Serial I/O	3P+S	3P+S	3P+S
Tape Cassette I/O	CUTS	CUTS	CUTS
Memory	**4KRA**	**8KRA**	**16KRA**
Price	$594	$730	$964

NOTE: The GPM module with both RAM and PROM is included FREE in all the above subsystems. The GPM kit is $129 if purchased separately.

The ALS-8/ROM chip set is $159. SIM-1 & TXT-2/ROM add-on set is $60 and requires both GPM and ALS-8/ROM.

I want Subsystem "B" to get my Altair or IMSAI up and running.

☐ Enclosed is a check for $_____.
California residents add 6% sales tax.
No shipping charge.

☐ Mastercharge # _____
(include Interbank No. and expiration date)

☐ Send more information

I want:
☐ B70 at $594
☐ B110 at $730
☐ B190 at $964

Name _____

Address _____

City _____ State _____ Zip _____

Processor Technology Corporation

6200 Hollis Street, Box G
Emeryville, CA 94608 (415) 652-8080

format of the papers to be printed in the Proceedings. Final papers will be due on May 1, 1977.

Registration information may be obtained from: CSE Workshop, P.O. Box 639, Silver Spring, Maryland 20901, (Phone: 301-439-7007).

TRENTON COMPUTER FESTIVAL

The Second Trenton Computer Festival will be held at Trenton State College, Route 1, Trenton, N.J. from April 30, 1977 to May 1, 1977. Featured are a special conference sponsored by IEEE on consumer and hobby applications of microcomputers, exhibits, displays, contests, a huge flea market for hardware and software and manufacturers' booths.

General registration is $4.00 with a special students' rate of $2.00 and sales $2.00 per spot. For advanced registration or information call Jaci Di Paolo at (609) 771-2487 or write Trenton Computer Festival, Trenton State College, Trenton, N.J. 08625.

TAKE HOME A MICRO

WINTEK has announced the Spring schedule for their workshop, "HANDS ON MICROPROCESSOR SHORT COURSE WITH FREE TAKE HOME MICROCOMPUTER." Attendees receive a microcomputer to use at the workshop and take home when they leave. The take home computer has a 6800, RAM, PIA (parallel I/O), ACIA (Serial I/O), and ROM with Fantom-11 (which supports single step, break points, etc.), and is fully expandable to 65K. Course schedule is May 10-12, Lafayette, IN; May 24-26, Cleveland/ Akron, OH; June 7-9, Syracuse, NY; and June 21-23, Hackensack, NJ. Tuition is $495. WINTEK Corp, 902 N. 9th Street, Lafayette, IN 47904, Tel. (317) 742-6802.

COMPUTER WORKSHOP

Institute of Electrical and Electronics Engineers, Inc. (IEEE) will hold a computer science and engineering curricula tutorial and workshop at the Quality Inn, Fort McGruder, Williamsburg, Va. June 6 to 8, 1977.

Dr. Richard Merwin, distinguished educator and pioneer in the computer field will keynote the workshop on June 6. A day-long tutorial on how to implement and teach a microprocessor laboratory will be presented by Dr. Imsong Lee on June 8.

Advanced registration and hotel accomodation information available Quality Inn, Fort McGruder VA 23185. Other information available from Arrangements Committee Chairpersons Dr. Gerald Engel, Virginia Institute of Marine Sciences Gloucester Pt. VA 23062 and Dr. Norman Gibbs, College of William and Mary, Williamsburg, VA 23185.

UPIEEE-77

Moore School, University of Pennsylvania UPIEEE-77 is holding a workshop on Bench Programming of Microprocessors from June 10 to 12, 1977 at Moore School of E.E., 33rd and Walnut Streets, Philadelphia, Pa.

The purpose of the workshop is to develop efficient methods of designing and troubleshooting microprocessor-based systems with using expensive assist equipment. Some of the subjects covered will be Procedures for Bench Programming, Microcoding, Assist Hardware, Debugging and Troubleshooting, Chip Evaluation and more.

A substantial discount can be obtained if you register before May 6, 1977. For registration contact Miss Helen B. Yonan. Moore School, IEEE, Univ. of Pennsylvania, Philadelphia, PA 19104 or call 215 243-8106.

NEW COMPUTER CLUBS

We wish to welcome another one of our friends from Canada, The Société d'informatique Amateur du Québec (S.I.A.Q.). This club is going to represent the area of Québec City in the province of Québec. We are very interested in the new clubs which are now forming and invite these clubs to send us a letter stating their general meeting places, agenda, and dates of upcoming meetings.

Also this month we wish to introduce the TIT TAT COMPUTER CLUB from Kitsap County in the state of Washington. Those of you who do not live on the peninsula are also invited to attend their meetings. Further information concerning club dates may be obtained by calling (206) 876-9050.

UPCOMING COMPUTER SHOWS

Apr. 5-7, 1977 **COMPUTER CARAVAN '77**
Los Angeles Convention Center. Three days of seminars and exhibits. Forums will take place from 9AM to 1PM. Exhibits will be open from 10AM to 5PM. There will be no charge to enter the exhibit hall.

Apr. 6-8, 1977 **MICROCOMPUTER-77**
Lincoln Plaza Forum. Oklahoma, City, OK. Contact Dr. S. C. Lee, School of Electrical Engineering, University of Oklahoma, Norman, OK 73019.

Apr. 15-17, 1977 **THE FIRST WEST COAST COMPUTER FAIRE**
San Francisco Civic Auditorium. A conference and exposition on personal and home computing. For further details contact Mr. James Warren, Star Rte. Box 111, Woodside, CA 94062, (415) 851-7075.

Apr. 19-21, 1977 **ELECTRO '77**
Convention Center, New York City, NY. Contact Joseph Antonaccio, convention manager, Electro '77, c/o IEEE, 345 E. 47th St. New York City, NY 10017.

Apr. 19-21, 1977 **COMPUTER CARAVAN '77**
Cleveland Convention Center. Three days of seminars. Free admission to exhibit areas.

Apr. 26-28, 1977 **COMPUTER CARAVAN '77**
St. Paul Civic Center, St. Paul, MN.

Apr. 28, 1977 **CALIFORNIA COMPUTER SHOW**
Palo Alto, CA. Featuring the latest in computer systems and peripherals for both the OEM and end-user markets. For information or show invitations, contact Norm DeNardi Enterprises, 95 Main St., Los Altos, CA 94022, (415) 941-8440.

Apr. 30 through May 5, 1977 **NEWCOM '77**
Las Vegas, NV. A series of meetings and conferences to be held Apr. 30 to May 2. Exhibits, conferences, clinics, and forums will be held from May 3-5. Further information may be obtained by writing: Electronic Industry Show Corp., 222 South Riverside Plaza, Suite 1606, Chicago, IL 60606. Phone (312) 648-1140.

May 3-5 **COMPUTER CARAVAN '77**
McCormick Place, Chicago, IL. Forums and free exhibits. For further information and registration procedures, write Computer EXPO '77, 797 Washington St., Newton, MA 02160. Phone (617) 965-5800.

May 10-12, 1977 **COMPUTER CARAVAN '77**
New York Coliseum, New York City, NY. Hundreds of exhibits, products and services will be shown along with computer user forums.

May 17-19, 1977 **NEPCON EAST**
Philadelphia Civic Center. Exhibitor conferences and products will be featured. For more information call Mr. Frank L. Buccaro at (312) 263-4866

May 24-26, 1977 **COMPUTER CARAVAN '77**
Philadelphia Convention Center. (See the May 3 calendar listing in this issue for details.)

May 31 through June 2, 1977 **COMPUTER CARAVAN '77**
Sheraton Park Hotel, Washington, D.C.

June 7-9, 1977 **COMPUTER CARAVAN '77**
Northeast Trade Center (Rte. 128, Exit 39) Boston, MA.

June 13-16, 1977 **NATIONAL COMPUTER CONFERENCE**
Dallas, TX. For information on the 1977 National Computer Conference contact Dr. Portia Isaacson, University of Texas, P.O. Box 688 Richardson, TX 75080.

INTRODUCING THE COMPLETE CHALLENGER SYSTEM.

OSI's DREAM MACHINE is a totally integrated computer system.

Imagine a system complete with terminal, CPU, memory, floppy disk, software, and all the little necessities to make it work together immediately. Now imagine this complete system available not only fully assembled, but priced much lower than anyone else's kit. What you are dreaming of is OSI's "new" Challenger System!

In the configuration shown above, the Challenger includes everything an end user needs for a complete small computer system. All you add is 110 VAC power and a desk to put it on.

This fully-assembled system includes:

HARDWARE:

OSI Challenger 65 with 16K RAM, serial interface, system monitor PROM, and floppy disk bootstrap PROM.

OSI Challenger single drive floppy disk formatted for 250K bytes storage per diskette surface.

Stand-alone terminal and Sanyo monitor for 16 lines of 64 characters at 2400 baud (other terminal options are available).

And all interconnecting cables!

SOFTWARE:

2 diskettes containing over 100,000 bytes of software including OSI's powerful Disk Operating System with variable length sectors. **6502 DISK BASED RESIDENT ASSEMBLER/EDITOR!** A totally interactive Assembler/Editor which assembles up to 600 lines a minute and is completely compatible with MOS Technology's Cross Assembler format. This program also contains a powerful disk-based line editor with commands for general text editing. **OSI'S EXTENDED MONITOR:** A powerful machine language debugging and utilities package including a Disassembler which is format compatible with the Assembler! **OSI 6502 8K BASIC FOR DISK BY MICROSOFT:** This powerful BASIC has all the features of Altair® 8K BASIC for the 8080 plus higher speed and disk storage. And it comes complete with a BASIC program library.

DOCUMENTATION AND SUPPORT:

We include over 600 pages of hardware, software, programming, and operation manuals. The Challenger is based on the well-proven OSI 400 system. The over 2,000 OSI 400s and Challengers now in use assure continuing hardware and software support for this system for years to come!

EXPANDABILITY:

The Challenger System can now be expanded to 192K of RAM and 16K of I/O and ROM. There are over 13 accessory boards including A/D, D/A, parallel and serial I/O, cassette interfaces, a dual drive floppy, a video graphics display, several RAM and PROM boards, and multiple-processor configurations.

APPLICATIONS:

The Challenger system is complete, fully assembled and configured so that the Disk Operating System can be booted in immediately on system power-up. Even a relatively inexperienced operator can have a complex BASIC program on-line just seconds after the system is turned on. The ease of use, high reliability, and large library of standard BASIC applications programs make the OSI Challenger System the first practical and affordable small computer system for small business, educational institutions, labs, and the personal computerist.

PRICES:

Challenger System, complete as stated above with terminal and monitor **$2599.00**

As above without terminal. Specify RS-232 or 20ma loop and baud rate **$2099.00**

IMPORTANT NOTE:

One of the most important features of the Challenger System is that it is not really "new". OSI has been delivering the basic circuitry of the Challenger since November 1975 and the floppy disk since June 1976. The only thing new is the total integration of the components as a complete, simple to use, fully-assembled, small computer system.

For more free information and the address of the OSI Computer Dealer or representative in your area, write to: OSI; Dept. S; Hiram, Ohio 44234 or enclose $1.00 for the full OSI catalog which contains kits from $134 and fully assembled computers from $439.

OSI

Ohio Scientific Instruments

11679 Hayden Street, Dept. S, Hiram, Ohio 44234

CALENDAR

Apr. 8 Panhandle Computer Club meets at Amarillo Junior College, Amarillo, Tx, at 6:30 PM in the Electronics Department. Those interested may call Tex Everett at (806) 373-8207.

Apr. 8 Crescent City Computer Club meets at the Lakefront Campus of the University of New Orleans at 8 PM. Call or write Bob Latham at (504) 722-6321 or P.O. Box 1097, New Orleans, LA 70122.

Apr. 9 Oklahoma Computer Club meeting at the Bell Aisle Library in Oklahoma City at 10 AM. Call Al Campbell at (405) 842-4933 or Don Coulson at (405) 722-0906.

Apr. 10 South Eastern Michigan Computer Organization (SEMCO) will meet at the studios of WJBK TV-2 at 6 PM. For further information, call club president Dick Wier at 565-3228.

Apr. 14 Rochester Area Microcomputer Society (RAMS) meets at 7:30 PM at the Rochester Institute of Technology, Bldg. 9, Room 1030, Rochester, NY. For further information write RAMS, P.O. Box D, Rochester, NY 14609.

Apr. 15 Long Island Computer Association will meet at the New York Institute of Technology, Bldg. 500, Room 508, Old Westbury, NY. Call (516) 938-6769 for club details.

Apr. 15 Homebrew Computer Club will be meeting at the Stanford Linear Accelerator Center Auditorium at 7 PM in Menlo Park, CA. Call Bob Reiling at (415) 967-6754 or write to P.O. Box 626, Mountain View, CA 94042.

Apr. 16 South Central Kansas Amateur Computer Association meets at 9 AM at 1430 E. Kellog, Wichita, KS. For further information write Chris Borger, 1504 N. St. Clair, Wichita, KS.

Apr. 19 Rhode Island Computer Hobbyist (RICH) Club. At press time no specific meeting place or time was available. Please write Roger Garrett, 16 Grinnell St., Jamestown, RI 02835.

Apr. 20 Northwest Computer Club will meet at 7 PM at the Pacific Science Center, Room 200, located at 2nd Av., N. Seattle, WA.

Apr. 21 Space Coast Microcomputer Club will meet at the Merritt Island Library Merritt Island, FL at 7:30 PM. Contact Ray O. Lockwood at (305) 452-2159 or Glenn Seaton at 784-1419 for club agenda.

Apr. 21 New York Amateur Computer Club will meet at 7 PM. Call Bob Schwartz at (212) 663-5549 for meeting place.

Apr. 24 Chicago Area Computer Hobbyist Exchange (CACHE) is meeting at the NIGAS Bldg., on Schermer Rd. in Glenview, IL at 12 PM. Call Bill Precht at (312) 620-1671 for further information.

Apr. 26 Sacramento Microcomputer Users Group (SMUG) meets at 7:30 PM at the Sacramento Municipal Utilities Dept. Training Bldg. located at 59th St. between R and S streets.

Apr. 28 Small Computer Engineering Association of Minnesota (SCEAM) will be meeting at 7 PM at 3010 4th Av. South Minneapolis, MN, near Lake St. and S. Nicollet Av. Call (612) 824-6406 for club agenda.

Apr. 29 Panhandle Computer Club will be meeting at 6:30 PM in the Electronics Department of the Amarillo Junior College, Amarillo, TX. Please contact Tex Everett at (806) 373-8207 for club details.

Apr. 29 Homebrew Computer Club meets at 7 PM at the Stanford Linear Accelerator Center Auditorium, in Menlo Park, CA. Call Bob Reiling at (415) 967-6754 for details.

May 1 North Orange County Computer Club (NOCCC) will meet at 12 PM at California State University, Fullerton. Signs will be posted at the administration building giving directions to the meeting. This month will also provide a Family Day and Software Swap Meet.

May 1 SCCS-Valley Chapter will be meeting at the Harvard School, 3700 Coldwater Canyon, Studio City, CA. Scheduled for May is a new products show sponsored by Signetics.

May 4 New England Computer Society, Inc. will meet at the Mitre Corp. cafeteria at 7 PM. Located on Rte. 62, in Bedford, MA. Contact Dave Day at (603) 434-4239 for details.

May 4 Northwest Computer Club will be meeting at 7 PM at the Pacific Science Center, Room 200 located on 2nd Av. in North Seattle WA. A graphics show is scheduled for this month.

May 7 Louisville Area Computer Club meets at 1 PM in the Speed Auditorium at the University of Louisville, KY. Details are available from Glenn Darwin at (502) 456-5589.

May 7 South Central Kansas Amateur Computer Association meets at 1430 E. Kellog in Wichita KS. Contact Cris Borger for details.

May 8 South Eastern Michigan Computer Organization (SEMCO) will meet at 6 PM at the studios of WJBK TV-2. Call president Dick Wier at 565-3228 for club agenda.

May 12 Rochester Area Microcomputer Society (RAMS) meets at the Rochester Institute of Technology, Bldg. 9, Room 1030 at 7:30 PM. For further details write RAMS, P.O. Box D, Rochester, NY 14609.

May 13 Homebrew Computer Club meeting will begin at 7 PM in Menlo Park, CA, at the Stanford Linear Accelerator Center Auditorium. Contact Bob Reiling at (415) 967-6754 for meeting details.

May 13 Crescent City Computer Club will meet at 8 PM at the University of New Orleans, Lakefront Campus. Call Bob Latham at (504) 722-6321 for details.

May 14 Oklahoma Computer Club will be meeting at the Belle Aisle Library at 10 AM. Call Al Campbell at (405) 842-4933 for the club agenda.

May 17 Rhode Island Computer Hobbyist (RICH) Club. Contact Roger Garrett at 16 Grinnel St., Jamestown, RI 02835, for meeting place and time.

May 19 New York Amateur Computer Club will meet at 7 PM. Call Bob Schwartz for meeting place at (212) 663-5549.

May 20 Long Island Computer Association meets at the New York Institute of Technology, Bldg. 500 Room 508, at 8 PM in Old Westbury, NY. Call (516) 938-6769 for further details.

May 21 South Central Kansas Amateur Computer Association meets at 9 AM at 1430 E. Kellog in Wichita KS. Call Cris Borger at (316) 265-1120 for club details.

May 22 Chicago Area Computer Hobbyist Exchange (CACHE) will be meeting at 12 PM in the cafeteria of the NIGAS Bldg. on Schermer Rd., Glenview, IL. Call or write to CACHE, P.O. Box 36, Vernon Hills, IL 60061 or (312) 620-1671.

May 24 Sacramento Microcomputer Users Group (SMUG) meeting will commence at 7:30 PM in the SMUD Training Bldg. on 59th St. between R and S streets. Write SMUG, P.O. Box 741, Citrus Heights, CA 95610.

May 25 Northwest Computer Club meets at 7 PM in Room 200 at the Pacific Science Center in N. Seattle WA.

May 25 Homebrew Computer Club meets at 7 PM at the Stanford Linear Accelerator Center Auditorium. Call Bob Reiling at (415) 967-6754 for details.

PRIME RADIX

ANNOUNCES THE **64K**™

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(and some very sophisticated state-of-the-art memory design)

65,536 BYTES

Your dream can be a reality with the Prime Radix Corporation's 64K™ memory system at a very cost-effective price. And because it is a standalone memory system, you've got the advantage of greater flexibility not ordinarily available from add-in memory. Some of the features are:

- The 64K™ is fully buffered, presenting one TTL load to the memory bus.
- The 64K™ is digital group bus and ALTAIR™ bus compatible. **When ordering, you must specify the bus architecture.** A plugcard and cable will be furnished for the particular bus architecture you specify.
- 64K™ is expandable to larger word lengths (16 bits; 24 bits; 32 bits; all organizations with or without parity). Other bus compatibilities will be available soon.
- The minimum complement of memory is 40K BYTES, with starting address locations at 0K, 8K, 16K, or 24K.
- The 64K™ comes assembled and tested with its own power supply, attractively housed in an aluminum cabinet, ready to plug into your system. With a choice of a freestanding cabinet or a 19" rack-mountable cabinet, 5"h x 18"w x 14"d.
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- Power/fail detection circuitry and battery backup will provide non-volatile memory (batteries are optional at extra cost).

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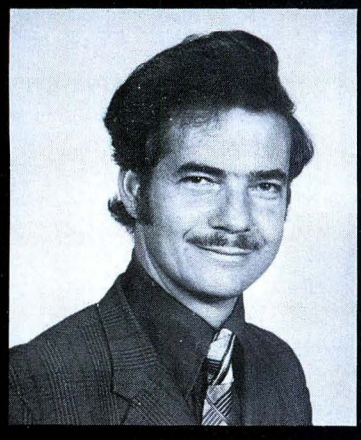
. . . FROM THE FOUNTAINHEAD

By Adam Osborne



The first small signs of a long predicted shake out are beginning to appear among microprocessor manufacturers. The first two casualties are the Elecronic Arrays EA9002 and possibly the Rockwell PPS-8.

The EA9002 simply took too long to develop. The smallest EA9002 system has three chips: The EA9002 CPU with read/write memory, external read only memory and I/O ports. In mid-1976 that still stood a chance of making it; but now, for simple applications, the EA9002 has to compete with the one-chip F8 from Fairchild and Mostek—and the 8048 from Intel. In more complex applications the EA9002 must compete with the two-chip 8085 system from Intel and the two-chip 6500 system from MOS Technology. Mark the EA9002 as the first stillborn 8-bit microprocessor.

Rockwell has not withdrawn the PPS-8, but they are no longer pushing it.

The demise of the PPS-8 is a sad story. Here is a microprocessor that appeared on the market early enough to compete with the 8080 and 6800—and capable enough to have won the race. But no one at Rockwell ever understood what they had, nor how to market it; and now it is too late. The PPS-8 has more support devices, and had them sooner, than the 8080 or the 6800; Parallel I/O, Serial I/O, Direct Memory Access Control, Priority Interrupt Control, CRT Controllers, Floppy Disk Controllers and Keyboard Controllers—the PPS-8 had them all before anyone else. So why did it fail? Because it has a strange instruction set. The PPS-8 uses "memory pools"; these are dedicated areas of memory where you can store instruction object codes, immediate data (for immediate instructions) and addresses (for subroutine calls). You place a subset of your instruction set in the pools, then you can have 1-byte immediate instructions and 1-byte subroutine calls. Your instruction now reads:

"Execute immediate instruction #3"

or:

"Execute subroutine call #5"

and the PPS-8 goes to the pool area of program memory to find out what these instructions are.

Now PPS-8 pools are supposed to save program memory; in theory this is possible since the pools allow you to have 1-byte immediate instructions, which normally have to be two bytes long, and 1-byte subroutine Call instructions, which are usually three bytes long. But to achieve this economy of memory requires a level of programming effort that costs more than you could conceivably save by generating shorter programs; memory is inexpensive. And the confusion of pooling proved too much for many programmers who were having a hard time coping with assembly language programming in the first place.

But what Rockwell never figured out for themselves, and never advertised, was the fact that data pools could be used *as a very powerful* way of letting external logic control the microprocessor. By implementing the pooled area of program memory in bidirectional I/O ports, external logic could control immediate data, addresses, and even instruction object codes—thus generating very compact and extremely powerful microcomputer systems for industrial process control applications. And that represents a much larger part of the microprocessor market than most people realize.

So if you think microprocessor manufacturers know what they are doing, you are wrong; everything that has happened so far has been the result of chance and happenstance.

Now that Rockwell are discontinuing the PPS-8 and Electronic Arrays are discontinuing the EA9002 what will they do instead?

Electronic Arrays will probably do nothing. They are a small company who does not need a microprocessor in the product line.

Rumor has it that Rockwell will second source the MOS Technology 6500 series of products; Synertek never was a very viable second source. Having Rockwell as a second source for the 6500 may be just what the 6500 needs; MOS Technology has always been short of funds and incapable of providing the hardware and software support that 6500 users would like. Rockwell do not have cash flow problems.

There is also a rumor running around that Rockwell are producing their own Super Z-80.

Motorola will be staying essentially with the 6800 for the next year.

There is a 6802 which is a two-chip 6800 system. The instruction set is identical; all that has changed is logic distribution. A 6801 due out at the end of this year will be a one-chip 6800, again with the same 6800 instruction set. The 6802 is supposed to compete with the new 8085 from Intel while the 6801 will compete with the 8048.

Complete Control.

Introducing IMSAI 8048 Single Board Control Computer.

Complete Control System
Intel developed the world's first single chip microcomputer. IMSAI has built the system to put it to work. Instantly!

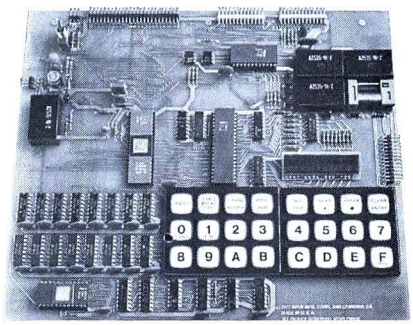
Presenting the IMSAI Single Board Control Computer. A complete programmable computer and hardware control system on an 8½" x 10" board.

Just plug in the power source (a 5V power supply or a 6V battery will do), and you can be controlling your home environment today!

The Chip Designed for Control
Intel designed the 8048/8748 single chip microcomputer with one thought in mind. Complete control. Everything you need is there: CPU, RAM, 1K ROM/EROM, I/O, timer/counter, interrupts . . . the works.

The Board That Implements It Instantly
There's a 24 pad hexadecimal keyboard and 9-digit LED hex display already on board. So you can start controlling the coffeepot and the sprinklers the minute you get the IMSAI home. Without adding anything but the connecting wires.

You can run almost any peripheral available. Not to mention the kids' electric train. The IMSAI Control Computer is



RS232 compatible. There are 12 quasi-bidirectional I/O lines with handshaking, and 14 more regular I/O lines, 5 heavy duty relays, and Teletype and audio cassette interfaces. All on one board.

There's already an extra 1K of RAM on board, plus sockets for another 1K of RAM and 2K of ROM/EROM. Still need more memory? The IMSAI 8048 allows expansion up to 64K of RAM off board.

Ultimately, the only limit to this system is your imagination.

Now, that's control.

For instant control, use the coupon provided.

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I want instant control!
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The only new upward compatible product which Motorola will introduce in 1978 is the 6809. This is going to be a 6800 with two or more Index registers and a somewhat improved instruction set. Details are not yet firm, but from what we hear, it certainly is a step in the right direction.

In my first column, I invited readers to telephone me if you have information that you think is interesting. My telephone number is (415) 548-2805. I extend the invitation again. So far the calls coming in indicate that there is need for some type of hobbyist "action line". Most callers are upset because they feel that when they bought their hobby computer hardware or software they did not get what they paid for. At the moment, I do not plan to take on the mantle of the computer hobbyist consumer advocate because it would do no good. Most of the companies catering to the computer hobby market are marginal organizations; the reason they do not always deliver what they promise is because they would go broke and deliver nothing if they did. So before you buy hobby computer hardware just remember that you pay for what you get. If you want solid and reliable hardware built to the highest engineering standards, go buy a minicomputer from Digital Equipment Corporation or Data General, and plan to spend 4 or 5 times as much money on it. Hobby computers are cheaper because the hobby computer manufacturers have cut corners. When you call the computer store with complaints, if you get no answer, it is not because they are trying to ignore you, rather it is because there is no one on the staff of the company whose job it is to listen to you; and when they start hiring the people to handle consumer complaints their payroll overheads will all increase.

Take your pick — do you want low cost or do you want service? You cannot have both.

Now as a hobbyist, if you wish to make sure that you get what you pay for, my only advice is that you buy products and not promises. Go down to your computer store and if you see it working in the store, buy it. If all you see is a brochure, don't buy it; chances are they will cash your check and spend the money to build the products.

While on the subject of new products, watch out for the floppy disc system with the truly ugly name: "Micropolis". Theirs will be the most sensibly-priced floppy on the market, and the guys who founded Micropolis are the same guys who founded Pertec. But for the ugly company name, they may have something; I wonder if the floppy will say "Kava Kava" every time it drops a bit.

Let us take stock of the software scene for the computer hobbyist.

Over the past year hobbyist magazines, including INTERFACE AGE, have done a superb job of printing source listings for a wide variety of imaginative and useful programs. In the beginning computer hobbyists distinguished themselves as thieves; they saw nothing wrong in copying programs for free, when they were legally supposed to pay a fee for the right to use programs. The result was that companies who planned to market software for hobbyists all went bankrupt in a hurry. But hobbyists have redeemed themselves by pitching in with large numbers of programs, all of which are donated free.

The only books of BASIC programs, up till now, have been ludicrously over priced and offer incompletely documented programs that frequently are less than advertised. I am planning to solve this problem during 1977 by publishing a series of low cost books describing general purpose programs, plus business application programs. Remember, a payroll program has more to it than calculating federal taxes based on gross income. There are a dozen different ways that people can be paid; but even that represents a small part of the problem. The really hard part of writing business application programs is coming up with complete operator dialogue schemes that second guess every silly thing an operator can do and give you easy methods of correcting erroneous data entry. File creation and maintenance is equally important. If your business application programs do not have adequate coverage in these areas, they are not adequate business application programs.

THE "FLOPPY ROM™" IS COMING IN THE MAY ISSUE!!

/ability.

It Comes Naturally With The Altair™ 8800b

The Altair 8800b from MITS: the second generation design of the microcomputer that started it all. The mainframe that has the abilities everyone is demanding from microcomputers today:

Expand-ability:

The Altair 8800b power supply and one-piece, 18-slot motherboard allow efficient and easy expandability for memory and I/O options. All Altair PC boards are designed to give you maximum capability/lowest power usage possible per board. This means that for each slot used you get more features and require less power, than with any of the "off-brand" Altair-bus-compatible boards.

Whether you buy an entire system up front or choose to expand gradually, it's easy to get the configuration you need with the complete family of Altair peripheral equipment, including floppy disk, line printer, audio cassette record interface, A/D converter, PROM programmer, serial and parallel I/O boards, choice of four different memory boards and many others.

Reli-ability:

The unique design features of the Altair 8800b, which have set the standard for the microcomputer industry, make it the most reliable unit of its kind. The Altair 100-pin bus, the now-standard design used by many imitators, has been "standard" all along at MITS. The unique Front Panel Interface Board on the Altair 8800b isolates and filters front panel noise before it can be transmitted to the bus. The all-new CPU board utilizes the 8080A microprocessor, Intel 8224 clock generator and 8216 bus drivers.

Flex-ability:

Meeting the diversified demands of an ever-increasing microprocessor market requires flexibility: not just hardware flexibility but software flexibility as well. MITS software, including the innovative Altair BASIC language, allows the full potential of the Altair 8800b computer to be realized.

8K ALTAIR BASIC has facilities for variable length strings with LEFT$, RIGHT$, and MID$ functions, a concatenation operator, and VAL AND STR$ functions to convert between strings and numbers.

Extended ALTAIR BASIC allows integer, single and double precision variables, automatic line numbering and renumbering, user-defined string functions, PRINT USING for formatted output and a powerful EDIT command for editing program files during or after entry. Extended statements and commands include IF . . . THEN . . . ELSE, LIST and DELETE program lines, SWAP variables and Trace On and Off for debugging.

Disk ALTAIR BASIC has all the features of Extended BASIC with the additional capability to maintain sequential and random access disk files. Utilities are provided for formatting disks and printing directories.

In all versions of ALTAIR BASIC you get the ease and efficiency of BASIC for the solution of real world problems.

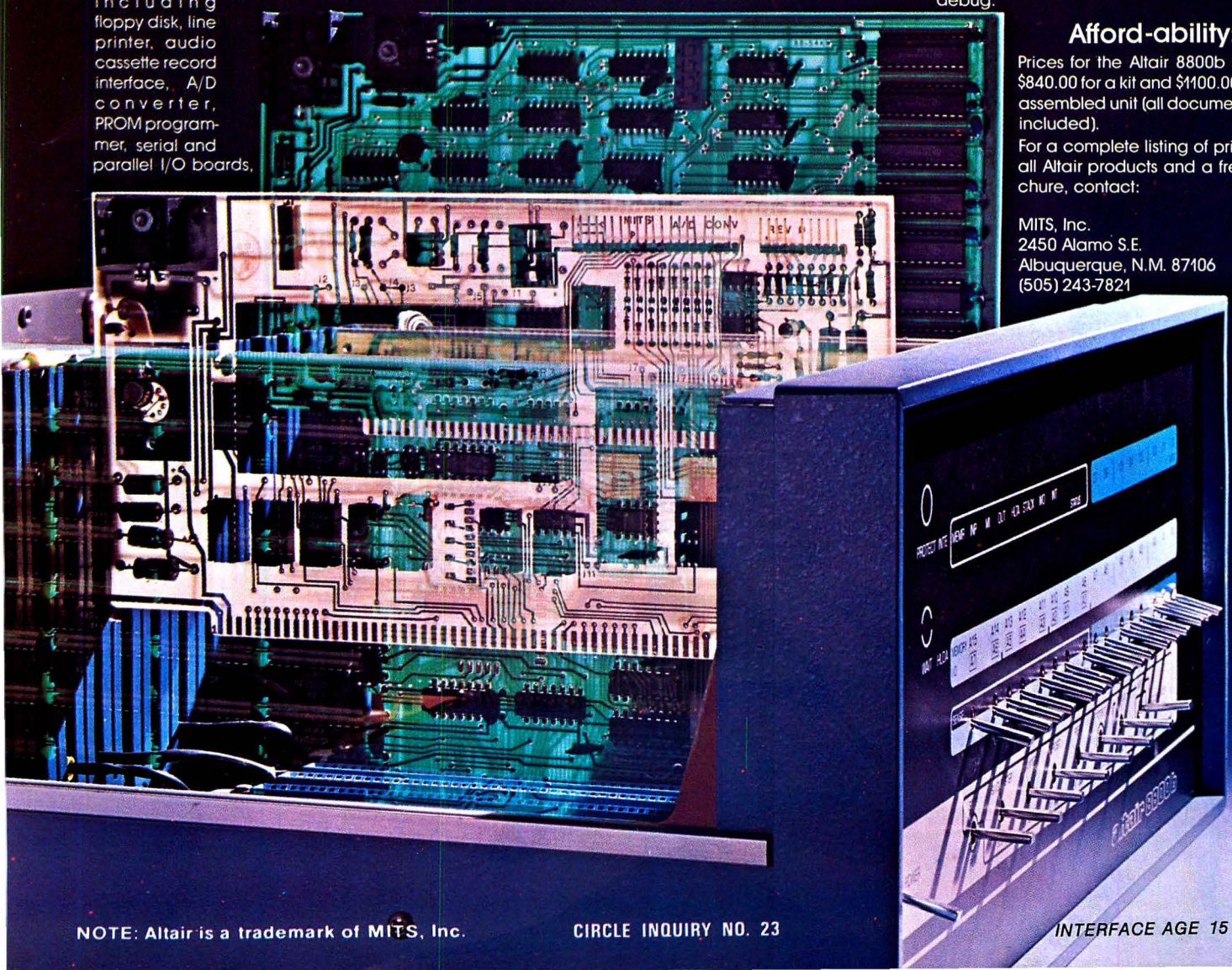
Package II, an assembly language development system for the Altair 8800b, includes system monitor, text editor, assembler and debug.

Afford-ability:

Prices for the Altair 8800b start at $840.00 for a kit and $1100.00 for an assembled unit (all documentation included).

For a complete listing of prices on all Altair products and a free brochure, contact:

MITS, Inc.
2450 Alamo S.E.
Albuquerque, N.M. 87106
(505) 243-7821



NOTE: Altair is a trademark of MITS, Inc.

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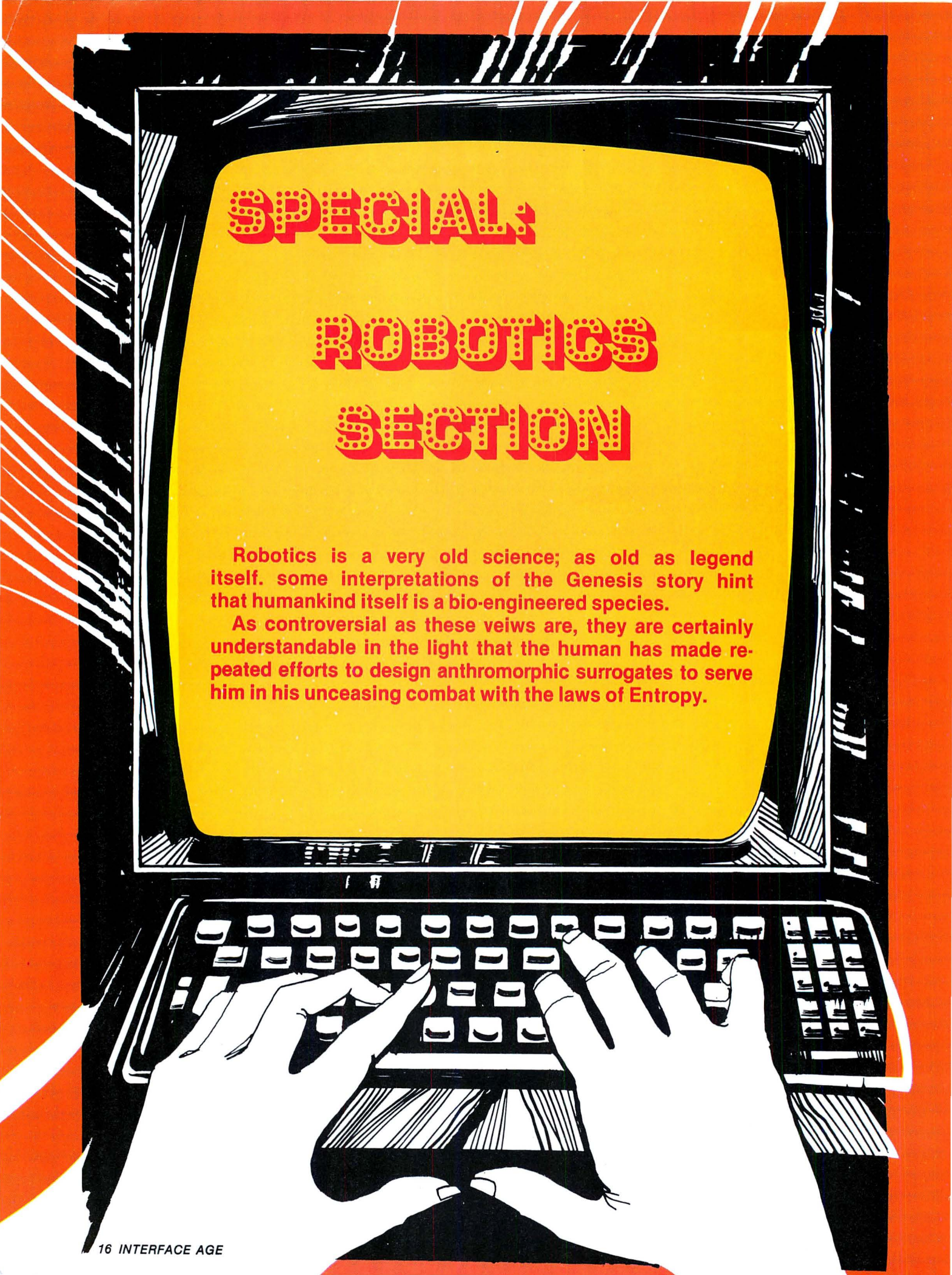

SPECIAL:
ROBOTICS
SECTION
Robotics is a very old science; as old as legend itself. some interpretations of the Genesis story hint that humankind itself is a bio-engineered species.
As controversial as these veiws are, they are certainly understandable in the light that the human has made repeated efforts to design anthromorphic surrogates to serve him in his unceasing combat with the laws of Entropy.

A Look at Robots

Partners, Puppets, Patrons or Pitfalls?

By Linda Folkard-Stengel, Associate Editor

The word *robot* is derived from a Slavic root meaning *work*. The first extensive mention of such a system comes from Mediaeval Prague where the semi-legendary Rabbi Loeb in the 12th Century is reputed to have built a humanlike servant to perform necessary household tasks on the Sabbath. We do not have detailed reports on the systems engineering employed by this ingenious scientist/theologian who created the GOLEM. We have only the report of his system of animation, couched in evocative cabalistic symbolism.

Rabbi Loeb gave "life" to his creation by stamping the Sacred Tetragrammaton on its forehead. On first hearing this sounds like alchemical gibberish until we remind ourselves that Hebrew letters also have numerical values. The Tetrammaton is formed by the יהוה (yod/he/vau/he) which carry numerical values of 10, 5, 6 & 5 respectively.

The next historical references on robotics are more concrete. They refer to the complicated clockwork figures called automatons. Although many were built in the 16th and 17th Centuries, the 18th Century marks the period when the art reached its peak. Many pieces exemplifying marvels of engineering and art are still extant.

With the maturing of the Industrial Revolution, the clockwork principles embodied in these beautiful toys found practical applications, and interest in automatons waned.

About this time a new concept took root: fear of man-made systems that would outgrow the limitations of their pre-designed purpose. The sensitive unhappy mind of Mary Wollestonecraft Shelley gave form to this fear in her novel "Frankenstein" and the cult has persisted to this day.

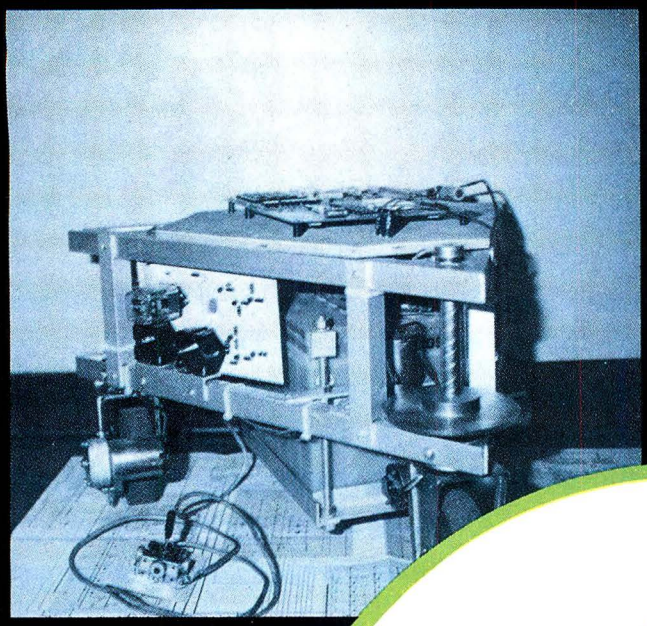
In this Century Dr. Isaac Asimov tackled the problem in his *I, Robot* series of science-fiction adventures published from 1940 onward in *Super Science Stories, Astounding Science Fiction* and later in book form by Doubleday and Signet. In that series Dr. Asimov formulated a fundamental code of behavior hard-wire-programmed into non-human thinking organisms. This code is THE THREE LAWS OF ROBOTICS which are:

1. A robot may not injure a human being, or, through inaction, allow a human being to come to harm.
2. A robot must obey the orders given it by human beings except where such orders would conflict with the First Law.
3. A robot must protect its own existence as long as such protection does not conflict with the First or Second Law.

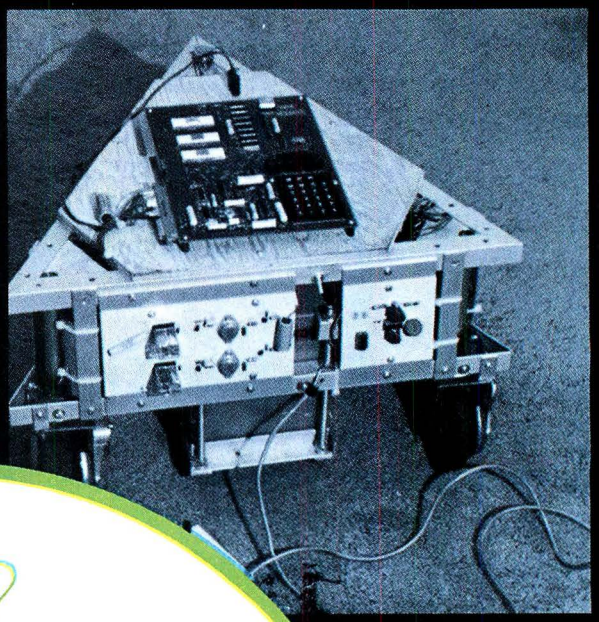
—Handbook of Robotics, 56th Edition, 2058 A.D.

Today the Era of the Microprocessor is upon us. As we see from Tod Loofbourrow's article and the many experiments in artificial intelligence, the Day of the Robot is dawning. That need not be a fearful event. With some preparation on the part of its human creator, the robot can be introduced as a valuable entity into the human community. Our children know this instinctively, and if they are supported in their enthusiasm for this playmate, the children upon maturity will shape this playmate into a useful servant to assist them to build a richer, more comfortable 21st Century.

Feature Stories in this Section



As long as I can remember I have wanted to build a robot.



.....how the robot should move around. I discarded the idea of legs.

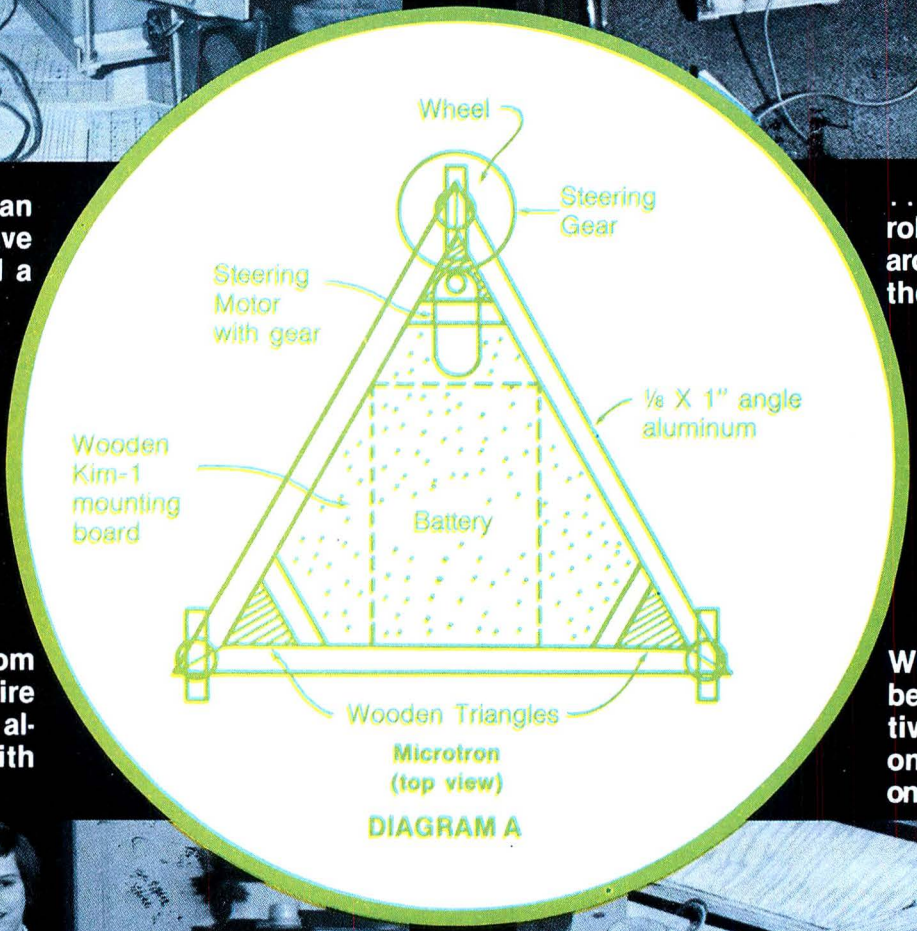
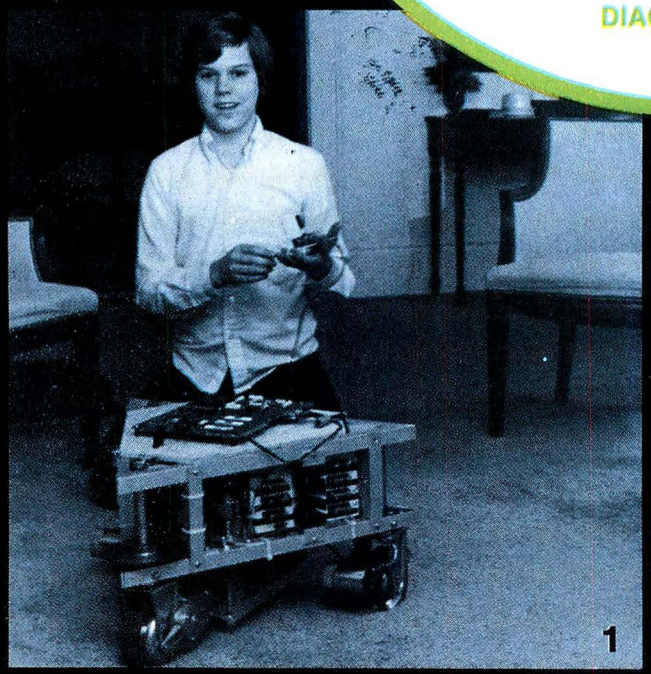


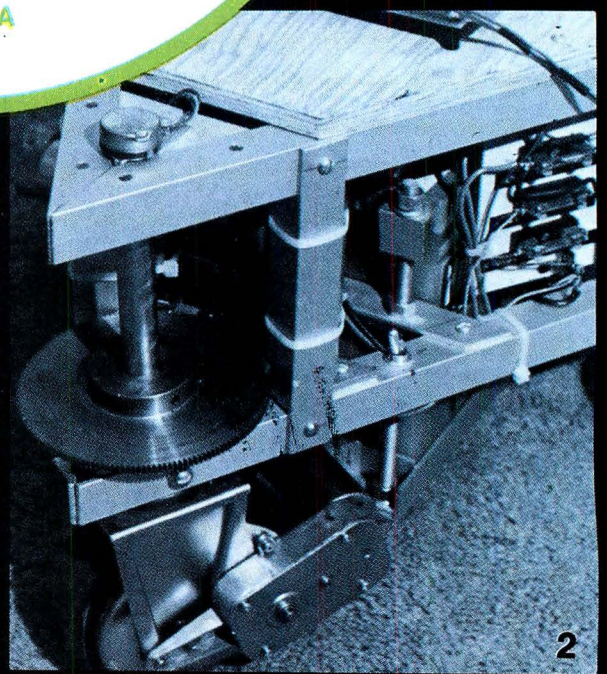
DIAGRAM A

I don't know from where this desire came, but it has always been with me.



1

Wheels seemed to be my best alternative. I decided upon a triangle with one steerable wheel.



2

ROBOTICS SECTION

A Computer Controlled Robot

by Tod Loofbourrow

Member of the Amateur Computer Group of New Jersey

Imagine the shock to some innocent passerby as he turns the corner in his morning jog and comes face-to-face with a speeding metal object. The object in question is Microtron, a triangular shaped robot that I built last summer when I was fourteen.[1] It is constructed of 1/8 x 1" angle aluminum and measures 15" in height and 23" per side.[A] Power for the robot is provided by a standard twelve volt car battery, channeled to three motorized wheels.

As long as I can remember I have wanted to build a robot. I don't know from where this desire came, but it has always been with me. I believe my first exposure to robots was at Montreal's Expo '67 where I saw a display of robots. Ever since then I have been fascinated by the idea of building such a device. Several times before I have tried and failed, the best of my efforts producing only a small empty metal box. Then last summer I came across a book about building a robot. Using the book as a guideline, I developed a mental picture of how I wanted the robot to look and then, I began to build.

My first decision to consider was how the robot should move around. I immediately discarded the idea of legs as being far too complicated, and not very fast. For a while thereafter, I was at a loss as to what to use. Wheels seemed to be my best alternative. I considered using electric window motors from automobiles and commercial wheels. The cost, however, would be high. I then came across a completely built motorized wheel in an electronics catalog.[2] Each reversible wheel was 4½" in diameter and 1" wide, and ran on 6 or 12 VDC. Individually, the wheels could carry a load of 200 lbs at walking speed on smooth, level surfaces. Stalled, these wheels had a pulling force of 20 lbs each. The current drain of one wheel was 2 amps with no load, and 8 amps stalled. These wheels appeared to be ideally suited for my concept of the robot, and so I designed it around them.

Requiring 12 volts to run the wheels at the specifications stated, I began to design a frame which could contain a 12 volt car battery. After trying many designs, I finally settled on a triangle both for stability and strength. A triangle also provided a good base for anything I might add, and it needed one less wheel than a rectangle or a square. The front wheel was to be the only steerable wheel, rotated by a separate motor, while the back two wheels were locked in place. A motor was, therefore, required to turn the front wheel. It happened that the same company that advertised the motorized wheels also had geared-down reversible motors. I ordered one of these at the same time as I ordered the motorized wheels.

When these materials arrived, I was able to construct a full-sized diagram of the finished frame and lay the parts out on it. I found that it had to be some 20" long. I immediately set to work building it, and in no time at all had the three wheels mounted in a sturdy triangular frame. It was then that I noticed that the wheels were not firmly anchored to the frame and could wobble. The reason for this problem was that the shafts coming up from the wheels were each set in a circular disk,

With the new microprocessors on the market, an inexpensive and more versatile alternative to hardware was available.

so that the wheels could rotate. The holes in the disks were slightly larger than the outside diameter of the shafts, giving a little play to the shafts. I had mounted the triangular frame on the outsides of the disks so that the wheels could rotate, hence the shafts wobbled too freely. The only solution I could see to this roadblock was to build a second triangle above the first and mount small wooden triangles in its corners. The shafts could then pass through holes in the wood. I built this second triangle and attached it rigidly to the first with pieces of angle aluminum. The wheels were then firmly mounted and, although they could still rotate, they were prevented from wobbling. The two triangles were separated from each other by five inches, and the entire framework was solidly bolted together. This new frame provided good support for anything I might add and was much sturdier than it was before the second triangle was added.

With the wobbling problem solved, I was able to mount my steering motor on the frame. Unfortunately, I ran into another problem. The steering motor, although geared down, was far too fast. It rotated the front wheel much faster than was necessary. This problem was easily solved by mounting a large gear on the shaft of the front wheel and a

1—See photo #1
2—See photo #2
A—See Diagram A

small one on the motor shaft.[3] The ideal gear ratio appeared to be ten to one. In other words, the larger gear had ten times as many prongs as the small one. When I first got the gears the hole in the larger one was only 5/8 of an inch in diameter. This was not a large enough opening for the 3/4" wide shaft to pass through. I, therefore, had to have the hole drilled bigger in a machine shop before I could mount it on the shaft. Once the hole was enlarged, I was able to mount the gear and hook up the steering motor.[A]

Now that the wheels and the steering motor were locked in place in the frame, I needed some way to contain the battery that powered them. My next step was, consequently, to design a battery cage. The first thing I did was lay a cross piece across the lower triangle of the frame 11" from the back. I bolted it in place. Second, I constructed a rectangle out of angle aluminum 12" long and 7" wide. The two shorter sides were turned so that the angle faced outward. The longer sides faced inward so that the battery could rest on them. All of it was held together by four 9" lengths of 3/8" screw rod, bolted in the corners of the rectangle. This screw rod was then bolted to the back of the frame and to the cross piece. It continued to extend above the top of the battery where small pieces of angle aluminum were bolted. The pieces of aluminum were to keep the battery from tipping. I then positioned the entire assembly so that it rode 2" above the ground. Once the battery cage was finished the main ribwork was complete and I could move on to the electronics of the robot.

As I built the framework of the robot, I had, at the same time, been building its circuitry. At first three main circuits were required to allow the robot to move and turn. The first of these circuits was a power supply.[B] This circuit took in +12 volts and by means of a regulator put out +5 volts. The +5 volts could be used for all other circuitry and for the computer which was to be added later. In addition, the power supply contained a series of fuses; it included a 7 amp fuse for the steering motor supply, a 20 amp fuse for the motorized wheels, a 1 amp logic supply fuse, a 7 amp regulator supply fuse, a 1½ amp fuse for the 5 volt supply to the computer, and a 1 amp fuse to supply 12 volts to the computer. The second circuit that I built was the motorized wheel control.[C] This circuit took in +5 volts and +12 volts and released +12 volts to go to the motor. It took in two TTL logic inputs, one for forward and reverse and the other to turn the motor on or off. The third circuit that Mike needed was a steering motor control.[C] Building the steering motor circuit actually consisted of constructing two identical circuits, one for turning right and one for turning left. Input for the steering control was +5 and +12 volts as was the input to the wheel control. The output was +12 volts. Two TTL logic inputs were required in addition, one to steer right and the other to steer left. All three of the circuits described above were bolted to the outside of the triangular frame, with all heat sinks snugly fitted to the aluminum. Altogether, the parts for the circuits cost under one hundred dollars. This fact got me to thinking about how much circuitry I wanted to add, and whether it would be cheaper to use a computer.

As soon as the inverter was added and the program perfected, Mike became a working robot.

With the new microprocessors on the market, an inexpensive and more versatile alternative to hardware was available. After due consideration I decided that a microprocessor would be my best choice, and in so doing opened up a whole new world. I looked around at several of the microprocessors and decided on the Kim-1. There were a number of factors that influenced my decision. One advantage was that the Kim was already built. Also it was lightweight and small, which was crucial since it was to be mounted on the robot. In addition, it was one of the least expensive microprocessors on the market, costing only $245.00. Of all the advantages, the one that was probably most important to me was that the Kim-1 came with its own built-in keyboard and display for loading programs. This fact meant that I didn't have to purchase an additional video or printer to load programs into the Kim.

I made up my mind to order a Kim-1. It took about two weeks to arrive and in the meantime I developed a mounting system for it. I cut a triangle out of ½" plywood 23" on a side. I then cut the ends off of the triangle five inches from each corner. This formed a rough hexagon that screwed down on top of the aluminum triangular frame. When the Kim-1 arrived I was able to mount it on ½" spacers and anchor it into the wood with screws.[4]

The first thing I did once the Kim was mounted was to load in and play a series of games. In spite of my fascination with these programs, I settled down to work. I read over the Kim programming language and with help from my father I began to face the problem of controlling the robot. The first step was to write a program. The best program appeared to be a program loop.* The computer would constantly be going through a series of instructions to monitor any commands given and then execute them. After getting the general program written, I found that three comparators were required to compare the input from the command pots with the actual position or speed of the wheels.[D] I tested the program with the comparators and then modified and perfected it. The final program loop could be subdivided into four parts for explana-

3—See photo #2
A—See diagram A
B—See diagram B
C—See diagram C

4—See photo #3
*—See flow chart and program
D—See diagram D

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tion purposes. The first part was the initialization, which was to get the computer ready to go through the main loop. The second section was the steering control, in which the computer compared the digital reading from the steering command potentiometer with a pot mounted above the shaft of the steerable front wheel. It then made the two numbers equal by rotating the front wheel right or left. A limit switch was written into the program so that the wheels can turn no more than 60 degrees in either direction.

The third part of the program was the speed control. The digital readout from the speed command pot was given to the Kim via a very simple analog to digital circuit. This number caused the computer to turn the motors on a specific number of time units out of ten, and off the remaining number of time units. The fourth part of the program was the speed and direction determination. This part of the program actually occurred before the speed control. The computer determined whether a command from the command pot was for "forward" or for "reverse" and then figured out at what speed. After the speed and direction determination part of the program figured out the number of "motor on" cycles out of ten, and the number of "motor off" cycles, the command was executed by the speed control section of the program.

Having perfected the program, I prepared to test it and, while doing so, I found a peculiarity with the Kim-1. When I hit the RESET button, instead of putting out logic zero on the output lines, as I had expected, the Kim-1 put out all logic 1's. This caused Mike to go into full speed forward, and if he hadn't been on a testing block he would have crashed headlong into the wall. This incident prompted me to add an inverter to Mike's circuitry so that the experience would not be repeated.[B] As soon as the inverter was added and the program perfected, Mike became a working robot. I wrote a few short programs so that when I was not controlling Mike, he would be moving about in a preplanned pattern. He moved in a clover leaf pattern for one of these programs, and for the other, executed a simple back-and-forth pattern, turning slightly left everytime it goes forward. These programs were used primarily for demonstration purposes and were not usually stored in memory.

After getting Mike working I controlled him at first with two potentiometers and a forward/reverse switch. One pot controlled the speed of the robot, while the other turned him right or left. Later I replaced this arrangement with a joystick.[5] All together, Mike had progressed from a whimsical idea in my head to a complex computer-controlled robot in less than three months.

Although Mike is a working operator-controlled robot, he is far more complete. He represents only the beginning of a complex *independent* unit. The next phase of construction will be to add some type of sensors to Mike's outer hull. First I will be wanting to add a framework over the triangle. I believe it will be in the shape of a nonequilateral octagon. On each side some type of sensor will

B—See diagram c
5—See photo #3

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be mounted, to detect wall or objects in Mike's path. I have experimented with the possibility of using proximity switches, but I have found them to be ineffective against wood and other non-conducting obstructions. Ultrasonics and infrared light offer two unrealistic possibilities because I do not have the knowledge nor the funds to employ either one. My most practical possibility is the use of bumpers. These bumpers could consist of metal plates mounted on buttons and springs. They could detect when Mike bumps into an object and make him respond according to which bumper was triggered. Any thoughts or suggestions about any other type of sensors would be more than welcome.

Besides sensors, there are many other additions I plan for Mike in the future. For one thing, when his battery gets weak, he will hunt out his charger and plug himself into it to recharge his battery. There is also the possibility that I will build up from his triangular base to give Mike two arms and a head. I may give him a voice or the ability to respond to certain voice commands. The possibilities are limited only by my imagination. Who knows? The next person you see walking down the street may, in fact, be something else. . . .

INITIALIZATION PROGRAM

```
0290  A9 1F   INIT  LDA #$1F     Set DDRA PA0-4 = OUTPUT
0292  8D 0117       STA $1701          PA 5-7 INPUT
0295  A9 00         LDA #$00     SET DDRB PB0-7 INPUT
0297  8D 0317       STA $1703
029A  A9 00         LDA #$00     LOAD A WITH 0
0296  85 02         STA $02      STORE IN SPEED COUNT
029E  85 03         STA $03      STORE IN 'ON' TIME
02A0  A9 0A         LDA #$ 0A    SET OFF TIME
02A2  85 04         STA $04      STORE IN 'OFF' TIME
02A4  A9 24         LDA #$24     SET STEERING TO CENTER
02A6  85 01         STA 01
02A8  A9 FF         LDA FF
22AA  8D 0017       STA 1700     SET PA TO ALL 1's.
02AD  A9 00         LDA #$00     SET BUMPER CYCLE
02AF  85 06         STA $06 =    COUNT TO 0
02B1  4C 35 02      JMP SCAN 3   START SCAN
```

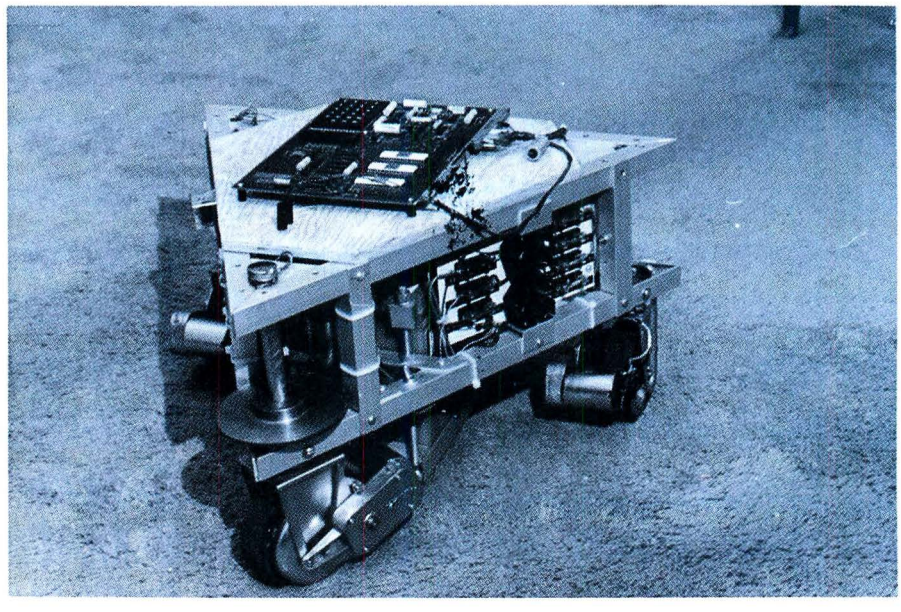
THIS ROUTINE HAS A MAIN PROGRAM WHICH IS PART OF THE MAIN SCAN ROUTINE. IT CONTROLS THE SPEED OF THE MAIN MOTORS BASED ON THE NUMBER OF TIME THROUGH THE SCAN ROUTINE.

SPEED CONTROL PROGRAM

```
02C0  A5 02   SCAN  LDA $02      GET SPEED COUNT
02C2  0A            ASL          SHIFT BIT 7 TO CARY
                                 (ON-OFF INDICATOR)
02C3  F0 05         BEQ CHNG     Branch if Speed Count = 0
02C5  C6 02         DEC $02      DECRIMENT SPEED COUNT
02C7  4C 0003       JMP SCAN1    Jump to Scan Continuation
02CA  B0 13   CHNG  BCS 0n       Branch if Carry Set ('ON' Cycle)
02CC  A5 03   OFF   LDA, $03     Get Value of 'ON' Time
02CE  F0 0F         BEQ ON       BRANCH IF VALUE = 0
02D0  09 80         ORA #$80     Add the "ON" Cycle Indicator
02D2  85 02         STA $02      PUT IN SPEED COUNT
02D4  AD 0017       LDA $1700    READ PA
02D7  29 F7         AND #$F7     SET PA3 TO '0' (Speed Control)
02D9  8D 0017       STA $1700    SEND PA3 = 0 (Speed Control)
02DC  4C 0003       JMP SCAN1    Jump to Scan Continuation
*CARRY SET—END OF ON CYCLE
02DF  A5 04   ON    LDA $04      GET VALUE OF OFF TIME
02E1  F0 E9         BEQ OFF      BRANCH IF VALUE = 0
02E3  85 02         STA $02      STORE IN SPEED COUNT
02E5  AD 0017       LDA 1700     READ PA
02E8  09 08         ORA #$08     SET PA3 TO '1'
                                 (SPEED CONTROL = OFF)
02EA  8D 0017       STA 1700     SEND PA3 = 1
02ED  4C 0003       JMP SCAN1    Jump to Scan Continuation
```

MANUAL CONTROL TABLE

```
0010  OF 0A   TABLE   FAST
0012  12 55           MEDIUM FAST
0014  17 73           MEDIUM                REV
0016  1D 82           MEDIUM SLOW
0018  23 91           SLOW
001A  26 A0           OFF
001C  29 91           SLOW
001E  2B 82           MED SLOW
0020  2D 73           MED                   FORWARD
0024  30 0A           FAST
0026
```



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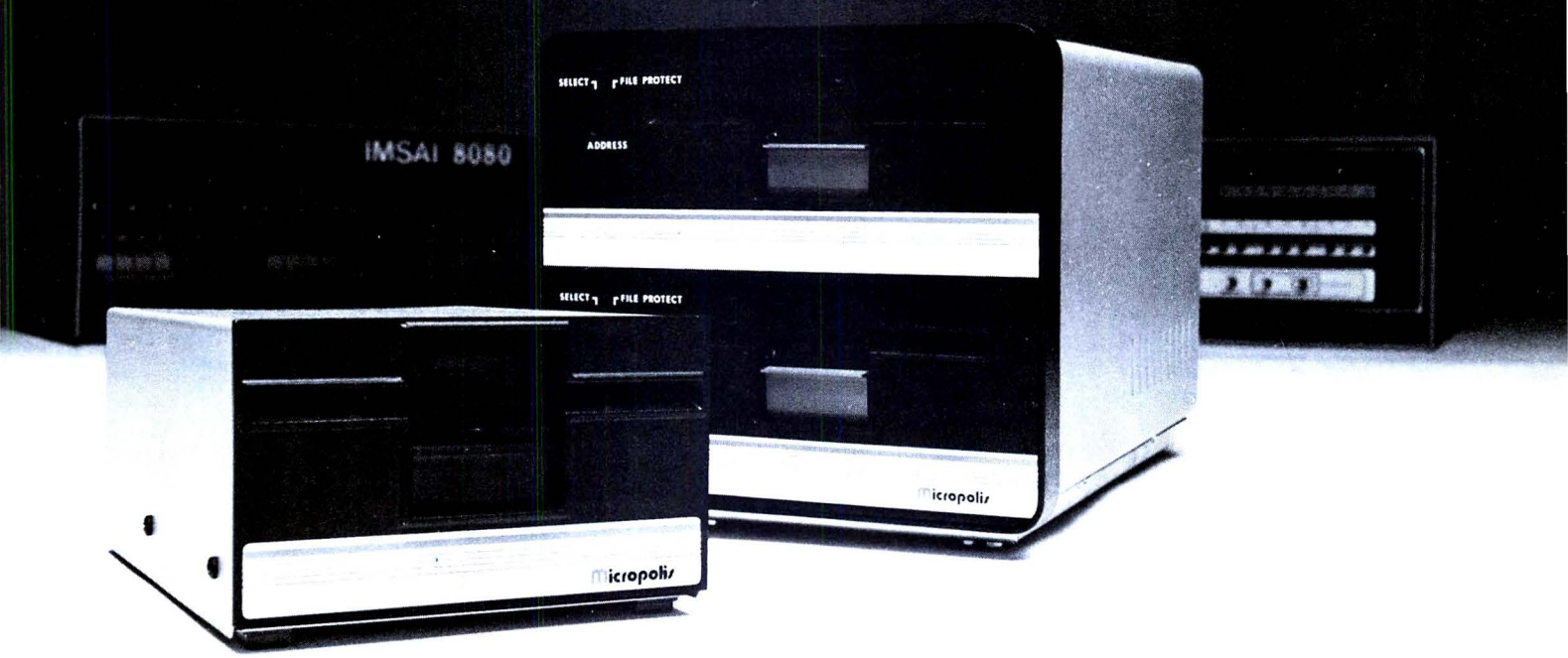

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```
Address  CODE      LABEL   MNEMONIC        COMMENTS

0200  20 IF 02  ATODI JSR START
0203  2E 00 17  L00PI  BIT 1700       TEST PA FOR INPUT
0206  10 FB           BPL L00PI      CHECK BIT 7 FOR '1'
0208  AD 00 17 STOP   LDA $1700      READ PA
020B  29 FE           AND #$FE       SET BIT 0 TO 0
020P  8D 00 17        STA $1700      OUTPUT '0' ON PA 0
0210  AD 04 17        LDA $1704      GET TIMER COUNT
0213  60              RTS

0214  20 1F 02  ATOD2JSR START
0217  2C 00 17  LOOP2BIT 1700        TEST PA FOR INPUT
021A  50 FB           BVC L00P2      CHECK BIT 6 FOR '1'
021C  4C 08 02        JMP STOP

021F  A9 42     START LDA #$42       STARTING COUNT
0221  8D 05 17        STA $1705      STOP COUNT IN -8 TIMER
0224  AD 00 17        LDA $1700      READ PA
0227  09 01           ORA #$01       SET PA0 TO '1'
0229  8D 00 17        STA $1700      OUTPUT A'1' ON PA0
022E  60              RTS
022D  A9 1F     MAIN  LDA #$1F       Set DDR PA0-4 OUTPUT
022F  8D 01 17        STA $1701            PA5-7 INPUT
0232  4C 58 02        JMP FQ                 INITIALRE
0235  20 00 02  Scan3 JSR ATOP1      GET  INPUT  1(Steering  Pot)
0238  85 00           STA #$00       Store Result in Save Area
023A  20 7D 02        JSR WAIT       Delay for Capacitor to Discarge
023D  4C 5C 03        JMP PATCH1     Go To Steering Limit Patch
0240  85 01           STA #$01       Store Result in Save Area
0242  20 7D 02        JSR WAIT       Delay for Capacitor to Discharge
0245  A5 00           LDA #$00       PUT LOC 0 IN ALL

0247  E5 01           SBC $01        Sub #IN LOC 1
0249  F0 0F           BEQ EQ
0248  10 18           BPL PL
024D  AD 00 17        LDA 1700       READ PA
0250  09 04           ORA #$04       Set PA2 TO '1' (Steer Left)
0252  29 FD           AND #$FD       Set PA1 to '0' (No Steer Right)
0254  8D 00 17        STA 1700       OUTPUT PA1 = '1' PA2 = '0'
0257  4C 72 02        JMP CONT       CONTINUE SCAN ROUTINE

025A  AD 00 17 EQ     LDA $1700      READ PA
025D  09 06           ORA #$06       Set PA1, PA2, to '1'
                                     (Left, Right Stay)
025F  8D 00 17        STA $1700      SEND PA1, PA2 = 0
0262  4C 72 02        JMP CONT       CONTINUE SCAN ROUTINE

0265  AD 00 17 PL     LDA 1700       READ PA
0268  09 02           ORA #$02       SET PA1 to '1' (STEER RIGHT)
026A  29 FB           AND #$FB       SET PA2 TO '0' (No Steer left)
026C  8D 00 17        STA 1700       OUTPUT PA2 = 1, PA1 = 0
026F   AC 72 02       JMP CONT       CONTINUE SCAN ROUTINE

0272  4C C0 02 CONT   JMP SCAN       NORMAL LOOP BACK
0275
                      FOR TESTING ONLY
0272  A5 01      CONT  LDA 01         FOR TESTING ONLY
0274  85 FA           STA FA
0276  A5 00           LDA 00
0278  85 FB           STA FB         FB
027A  4C C0 02        JMP SCAN

027D  A9 28     WAIT  LDA #$28       Starting Timer Count (Check)
027F  8D 05 17        STA $1705      STORE IN -8 TIMER
0282  A9 00           LDA #$00
0284  CD 0417   Check CMP 1704
0287  D0 FB           8NE Check
0289  60              RTS
```

MANUAL CONTROL PROGRAM

Address	Code	Label	Mnemonic	Comments
02F0	20 1F 02	A to D3	JSR START	START A/D 3 COUNT
02F3	A9 20	LOOP3	LDA #$20	SET MASX FOR PA5
02FS	2D 00 17		AND $1700	
02F8	F0 F9		BEQ L00P3	BRANCH IF PAS = 1
02FA	20 08 02		JSR STOP	Stop A/D 3 Conversion A = Value
02FD	60		RTS	
02FE				
0300	20 F0 02	Scan1	JSR A TO D3	ON RETURN A = VALUE
0303	85 F9		STA $F9	PUT BYTE IN DISPLAY AREA
0305	C9 26		CMP #$26	IF VALUE > = 26 THEN
0307	10 2E		BPL REV	GO TO FORWARD ROUTINE
0309	AD 00 17		LDA $1700	
030C	09 10		ORA #$10	
030E	8D 00 17		STA $1700	SET PA4 = 1 (REVERSE)
0311	A5 F9	SCTAB	LDA $F9	Retrieve Byte From A/D 3 Conv.
0313	A2 00		LDX #$00	SET INDEX REG = 0
0315	D5 10 EA	Again	CMP Table, X	Get Table "Speed" Value
0318	30 06		BMI FOUND	Branch if Hit in Table
031A	E8		INX	
031B	E8		INX	INCREMENT TO NEXT VALUE
031C	E0 12		CPX #$12	CHECK FOR END OF TABLE
031E	D0 F5		BNE AGAIN	
0320	E8	Found	INX	Move Pointer to "Action" Value
0321	B5 10 EA		LDA TABLE, X	Get Action Value Into A
0324	4A		LSR	SHIFT LEFT 4 BITS
0325	4A		LSR	TO RIGHT—FILL IN
0326	4A		LSR	ON LEFT WITH 0's
0327	4A		LSR	
0328	85 04		STA $OFF	PUT VALUE IN OFF TIME
032A	B5 10 EA		LDA TABLE, X	GET ACTION VALUE AGAIN
032D	29 0F		AND #$0F	MASK OUT LEFT 4 BITS
032F	85 03		STA $ON	STORE IN "ON" TIME
0331	20 7D 02		JSR WAIT	Delay for Capacitor Discharge
0334	4C 35 02		JMP SCAN3	
0337	AD 00 17	REV	LDA $1700	
033A	29 EF		AND #$EF	
033C	8D 00 17		STA $1700	Set PA4 = 0 (Forward)
033F	4C 11 03		JMP SCTAB	NOW SEARCH TABLE

STEERING TABLE PATCH

035C	20 14 02	Patch1	JSR ATOD2	Get Count (Patch from 923D
035F	A2 00		LDX #$00	SET INDEX = 0
0361	DD 73 03	Again2	CMP TABLE 2, X	GET STEERING VALUE
0364	30 06		BMIFOUND2	BRANCH IF HIT IN TABLE
0366	E8		INX	
0367	E8		INX	Increment to next Value
0368	E0 14		CPX #$14	CHECK FOR END
036A	D0 F5		BNE AGAIN2	
036C	E8	Found2	INX	Move Pointer to Steering Val
036D	BD 73 03		LDA Table2,X	Get Steering Value into A
0370	4C 40 02		JMP 0240	RETURN FROM PATCH
0373	0E 26	Table2	0E 26	Table of Steering Values
0375	13 26		13 26	Left Byte is From
0377	18 27		18 27	A → D Conversion Right
0379	1D 28		1D 28	Byte is Value Used
037B	22 29		22 29	To Determine Steering
037D	27 2A		27 2A	Angle.
037F	2A 2B		2A 2B	
0381	2C 2C		2C 2C	
0383	2E 2D		2E 2D	
0385	3Q 2E		3Q 2E	
0387	31 2F		21 2F	

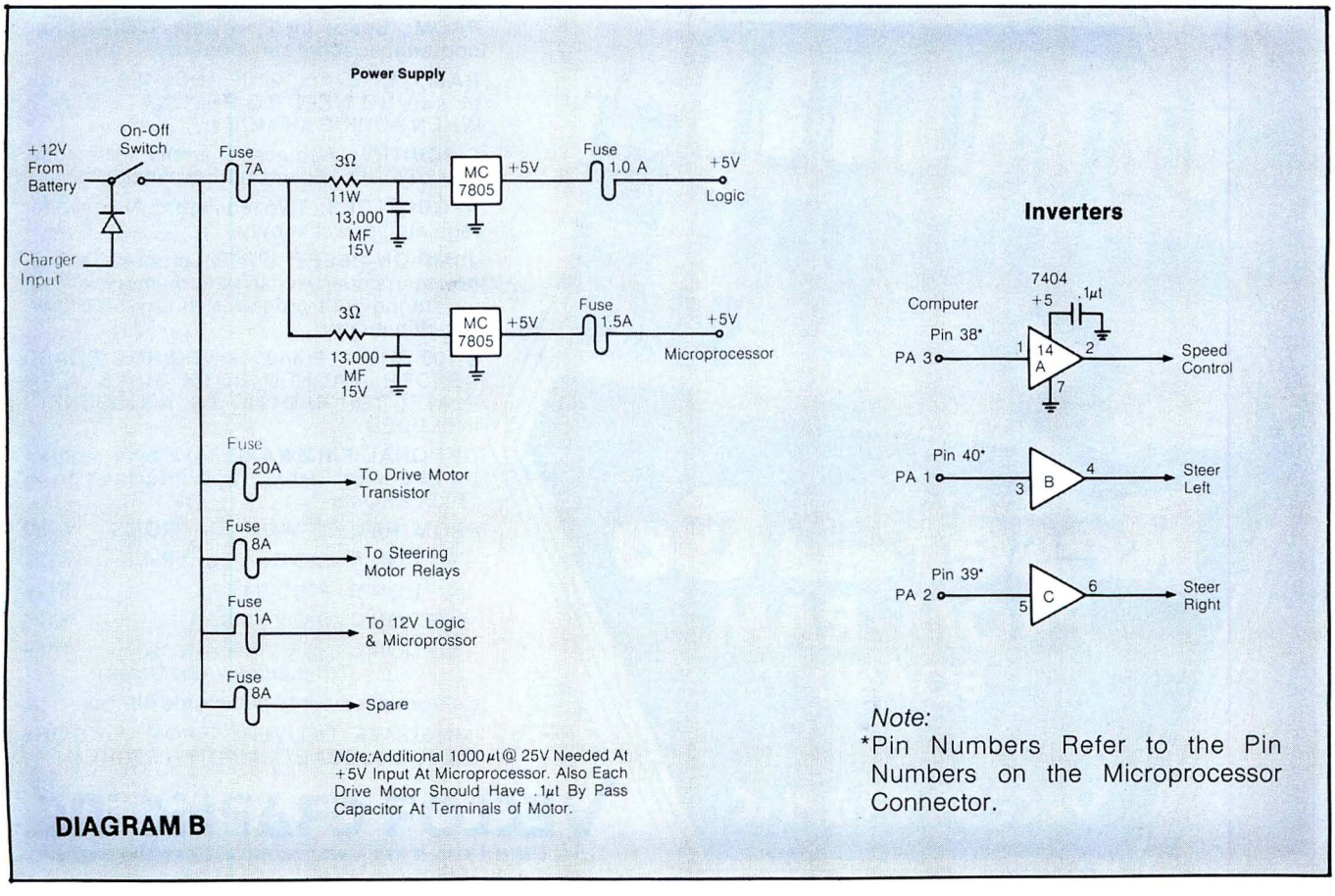


DIAGRAM B

Motorized Wheel Control

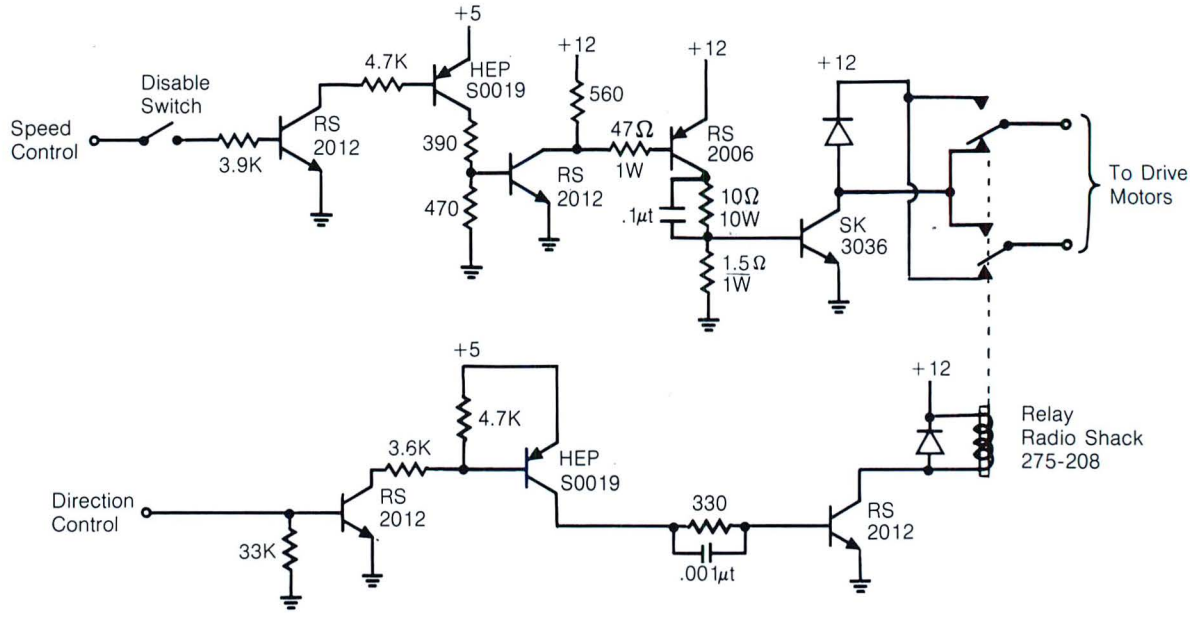
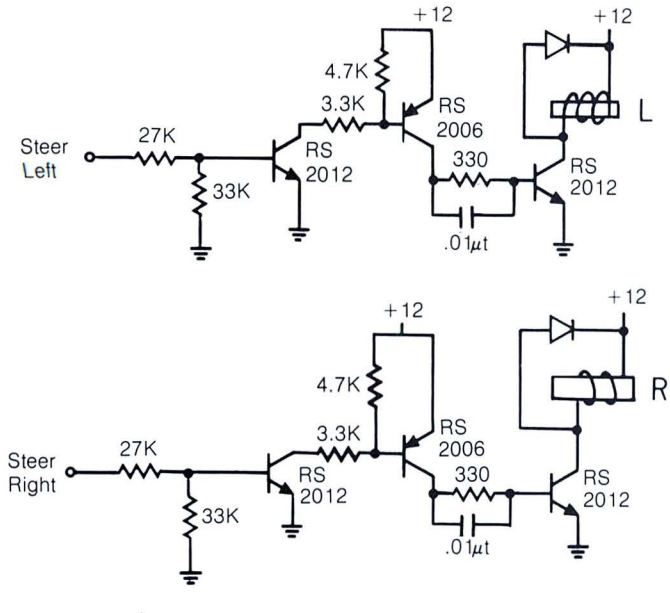
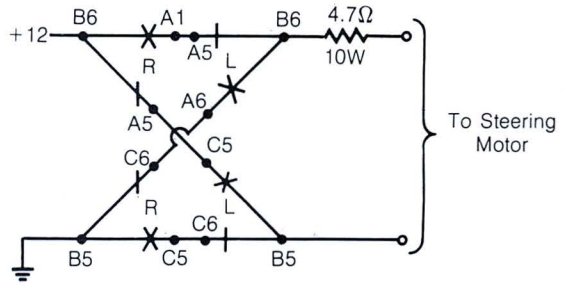


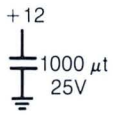
DIAGRAM C

DIAGRAM C continued

Steering Motor Control

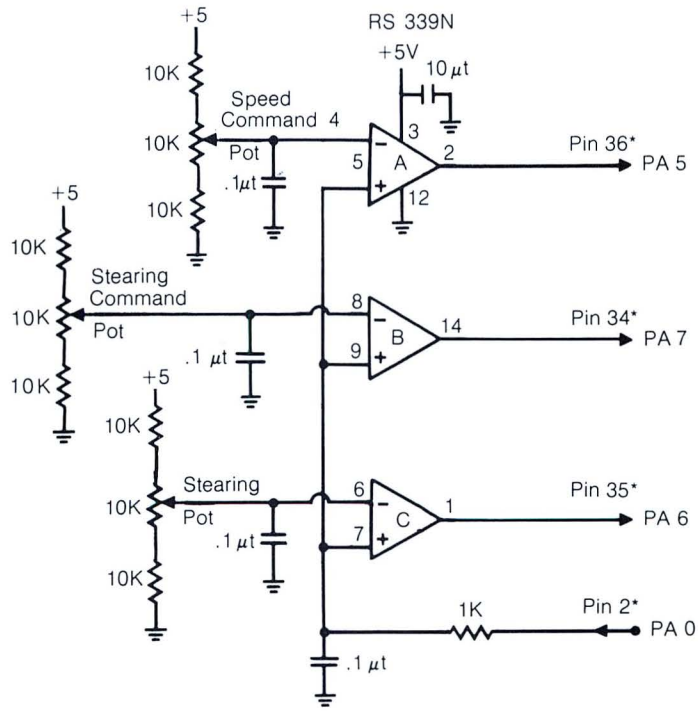






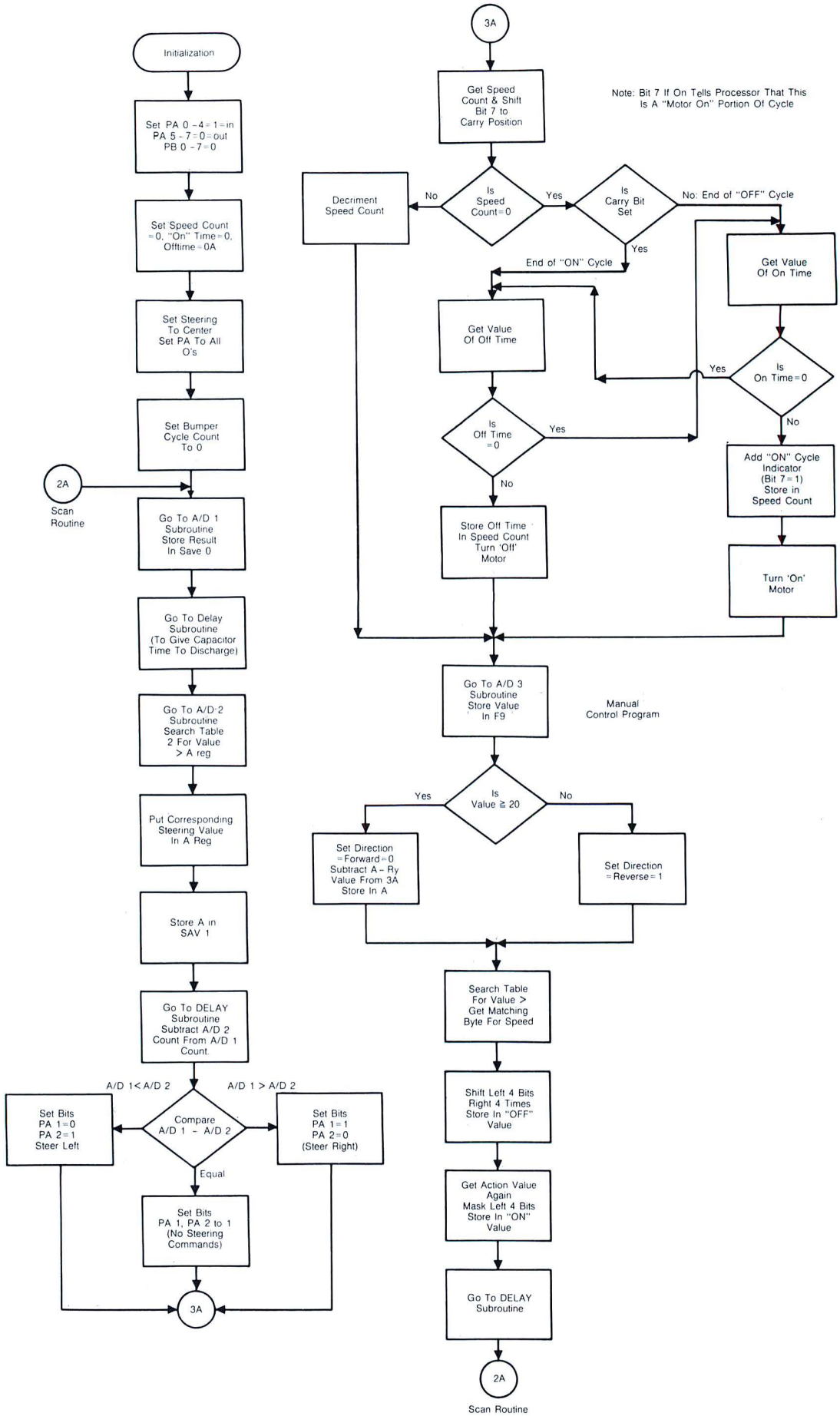
Note: "X" Represents The Normally Open Contacts & "1" Is The Normally Closed Contact.
Relay Contacts Shown For Radio Shack Relays Part #275-206

Comparators



* Microprocessor Connector

DIAGRAM D



Flow Chart for Joystick Control Program

L. E. D. FLASHER

(For Dasher—Or Any Other)

by Nathan Loofbourrow

FOREWORD—Nathan Loofbourrow is the seven-year old member of this gifted family. John, the child's father typed his notes and included them in the manuscript. We are so impressed with the achievement of this prodigious child that we have made a photo-montage of his notes as shown in Figure 3.

I got a L.E.D. Flasher Kit for Christmas. Here is how to make one. You need: a circuit board, a 555 timer, two 240 ohm resistors, one 2000 ohm resistor, one 750,000 ohm resistor, two L.E.D.s, and a 1.2 μfd, and 35 volt capacitor.

Connect them as shown on Picture #2. One L.E.D. is on and one is off. You will find more information when you build one. To run it, you need a nine volt battery.

On my circuit, one lights up a lot and one glows a little. Warning! . . . If a L.E.D. does not light up, do not replace a part unless you put in the L.E.D. both ways. Happy flashing!

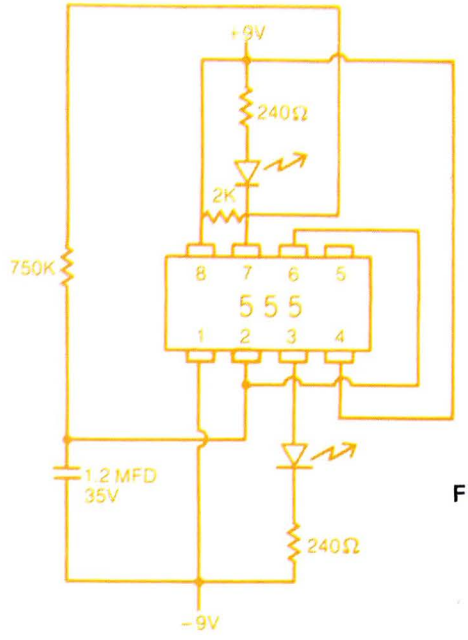


FIGURE 2.

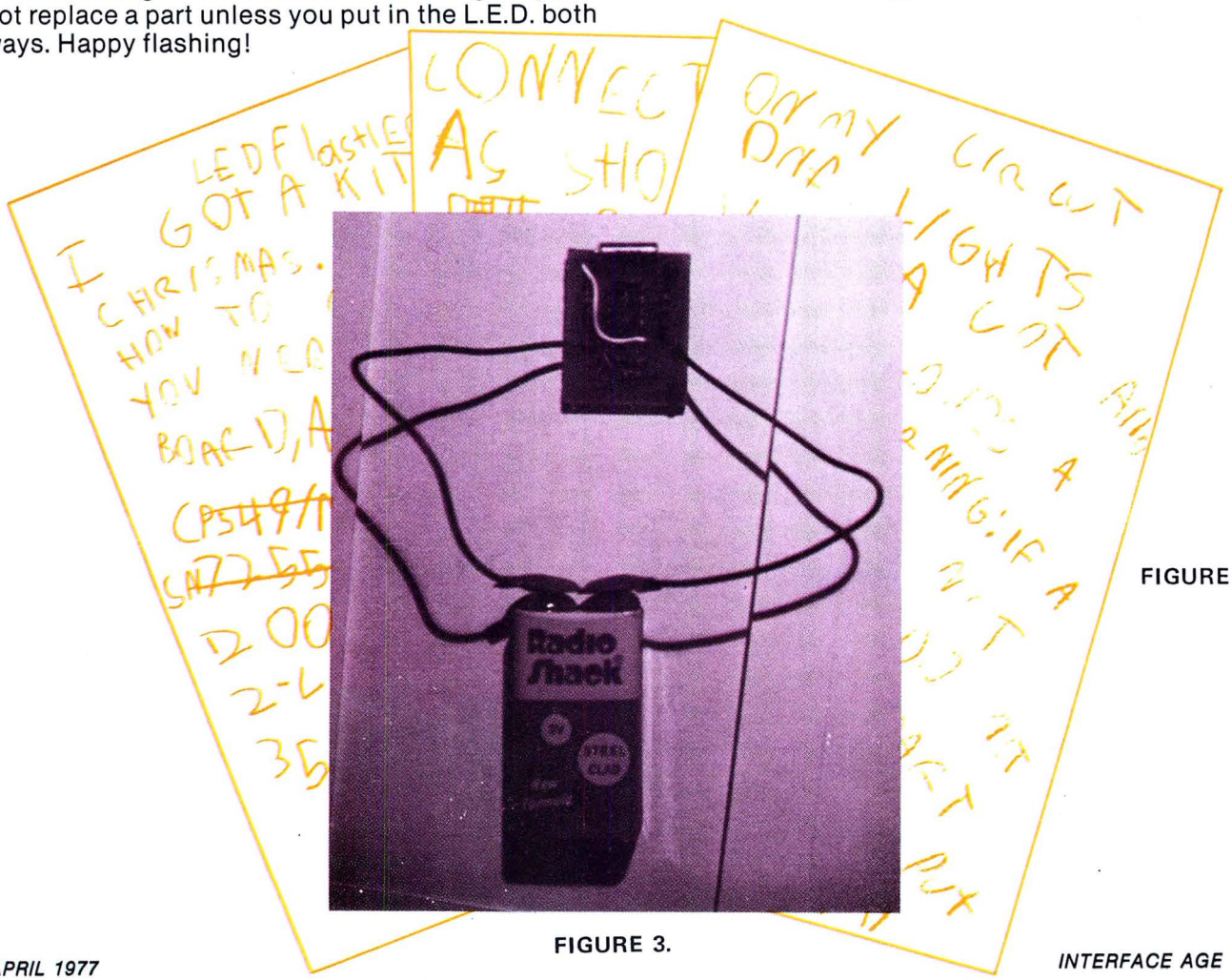


FIGURE 3.

FIGURE 1.

ROBOTICS SECTION

Robots As Household Pets

by Robert Rossum

Obviously, some decades must pass before we can expect any help from robots in driving buses, running city government, leading rescue teams to downed aircraft, and settling international disputes. In the meantime, more modest and, frankly, more interesting applications of robotics are possible. Robots are usually imagined first as domestic servants that will do household chores without complaining, but such capability calls for feats of mechanics and judgment now far beyond our practical resources. We can, however, build robots in the form of household pets to which people may become fondly attached. Although some people will be repelled by these creatures, this should not discourage us from pursuing robotics—many people are repelled by dogs and cats.

The first step is easy—we speculate on the characteristics of household pets and the practicality of building these characteristics into robots.

Consider cost. Assume that we're not interested in building just one or two toys for zealous, rich people, but in creating a product that can be distributed widely. What should it cost? Well, what does a pet cost? There's a range, to be sure, running from mutts that can be ransomed for a dollar from the dog pound up to rare, specialized pooches that have been developed over many generations of careful breeding, valued at several thousand dollars. Notice that the difference is not in the flesh, bone, and sinew, but in the *information* that goes with the dog. In general, the price rises with the sophistication, the information content, of any item being traded.

Size matters, too. Indeed, we have access to a study that allows us to gauge the probable acceptable price of any given item in our society, given its weight and sophistication. Notice that a microcomputer with a fair amount of memory, power supply, cabinet, and small keyboard weighs 15 to 20 pounds and sells for about a thousand dollars. You can buy 20 pounds of bread for much less than that.

Our pet robot cannot be picked up for a "buck" at the Robot Pound yet and it's obviously as sophisticated as a microcomputer. Its price, then is related to its weight also. How much should it weigh?

Since this pet is to live in the house, we must consider the weight of things that commonly live in houses. People live in houses. From the time they are first mobile to the time they are grown, they weigh somewhere between about 15 and 300 pounds. Their weight is distributed over a fairly large area on their big feet (and their hands and knees when they're small) so no great forces are brought to bear on small points, even when they stamp their feet or jump. Mobile household pets share these characteristics.

Few indoor pets weigh more than a hundred pounds. Few have such sharp, pointed hooves that they mar the floor. (Ladies with spiked heels are often encouraged to take their shoes off to avoid damage to hardwood floors and carpets.) Though some German Shepards live inside, most acceptable household pets are smaller, ranging from 15 to perhaps 50 pounds.

Judging from floor-loading characteristics and common practice, we're shooting for a robot pet that weighs 25 to 40 pounds. It's sophisticated, new, rare, but in detail not completely novel. Looking at our chart that plots the log of product weight against the log of price in dollars-per-pound for things in our society, such a product as ours should cost around a thousand dollars. If it sold for 10 times that much, it would have little practical chance of popularity. If it sold for a tenth of that, it would have little practical chance of being manufactured.

After cost and weight, what about velocity? Things that live around the house seldom move more than 5 miles-an-hour. If a little kid gets up to that speed, somebody shouts "Quit that running in the house!" If the dog moves that fast, he's chucked outside and if the cat does it, he's assumed to be having a crazy spell and he's fended off with a broom. Four mph is a very rapid walk for a man.

A pet that moves more slowly than .5 mph probably can't move fast enough to play with the kids. If it moves faster than 2 mph, it's considered too frisky. So, .5-2 mph for the robot household pet may be a good range.

What can the pet do physically? It had better not do very much. Monkeys with grabby hands are seldom allowed to roam homes freely. Dogs and cats are not encouraged to meddle with the things that people use. If they can push open a door that is ajar or pick up a newspaper when they are told, that's enough. No fondling of the dishes, the furniture, nor guests is acceptable. People don't want their pets to be capable to taking liberties with valued items.

If the pet robot can move about, that's probably enough. Refinements like the ability to climb stairs or to pick up small objects from the floor are probably desirable options, but that's a matter of important choice that is best left to the individual pet owner.

What about information content? In this case we do not want to simulate human behavior, but we must block out our objectives within the expected technological framework. We can usefully distinguish here between structure and logic. That is, the information content of a stone axe, for example, lies completely in its physical structure. It is useful for some things, not useful for others, and not at all adaptable. You can't make a silk purse out of a stone axe. Everything it "knows" is determined at the moment of its completion.

More sophisticated machines, however, are equipped with some logic, with structure or circuitry that "learns" from the environment in which it operates. An automatic record changer, for example, adapts to the size of the records it is handling, one at a time, and may be equipped with elaborate sensory and judgmental apparatus to vary its performance greatly with varying circumstances.

The pet robot must be able to do something, but not *too much*. Monkeys, dogs and cats are not encouraged to meddle with the things people use.

Our pet robot must have certain sensory and response capabilities as part of its basic structure. Certain pattern recognition capabilities are part of the structure of living things: a frog's eye (even when it is disconnected from the frog's brain) puts out a jolt of signal when something that looks like a fly crosses its field at a distance of a frog-tongue. That's the way the system is built. A human baby 15-minutes old, even before it has learned to "see" will turn to a crude portrayal of a human visage, away from other forms presented at the same time. That's the way the baby is built.

The pet robot, like the pet dog or cat, will have some such structural basic characteristics. What we add to that in the way of "logic"—the ability to learn from experience—is a matter of taste. Perhaps we should remark early and often that the key to maintaining a healthy relationship with the pet is to keep total control over its learning. You don't want someone teaching your parrot to say things that will offend you. You don't want your pet robot to learn habits that annoy or frighten you. The pet owner may have a key to the switch that turns the learning circuitry on and off and he may want to wear it like a dog tag around his own neck.

Of course, the pet robot can be "retrained" at any time, his memory utterly erased so that everything he has learned—bad habits and good—are eliminated. We'd hesitate to do that to a dog, but we don't mind rebuilding a machine, do we?

Without dwelling on this in a brief speculation, we may note that intelligence in animals seems to be related to the number of input channels to the brain, compared with the number of "thinking" cells in the brain—the ratio of nerve inputs to the number of neurons. An ant, which can learn just a little, but relies mostly on structural information for its operations, has a ratio of about one-to-one. In a rat, the ratio is about 18-to-one. In a human being, the ratio is about 500-to-one. What should it be in the pet robot? What *can* it be? There's room for a lot of discussion and experimentation here.

What must the pet robot *be like* to be welcome in the home? Again, what's welcome now?

Mammals are all roughly spherical in shape. When engineers calculate heat flow and the like for mammals, they can use a spherical model without being too far off. The pet robot may want to be roundish, with a density of about 1, the density of water, Most of a mammal's weight *is* water, which weighs 64 pounds per cubic foot. It may be difficult to package a 40-pound pet in a cubic foot, but remember that we may reasonably be off by a factor of two or three without exceeding practical tolerances.

All baby mammals have large eyes and high foreheads.

People regard little critters with these characteristics as desirable. Poodles are ordinarily trimmed to exaggerate the big eyes and high foreheads. Probably owls are the most popular artistic subjects among birds because of their mammalian appearance. All baby mammals are cuddly and non-threatening and people feel at east with them, while adult mammals make us all uneasy until we get to know them. Narrow-eyed bull terriers are "mean looking" dogs. Surely, the pet robot must have big, baby eyes and a high forehead to be welcome. Dark eyes, too. Why? Because angry, agitated people ordinarily have the pupils of their eyes stopped down to small apertures. Like the bull terrier, they look dangerous. Relaxed people, at ease with their surroundings, have large, dark pupils (except, of course, in harsh light) that put others around them at ease. Dark eyes are a sign of benign tranquillity in the ordinary world. To put people at ease, the pet robot wants large, dark eyes.

The pet robot must look like a friendly *mammal. It should* also smell like a friendly mammal—or like something of which people ordinarily approve. A new car smell? Musk? A soft pine smell bringing to mind furry forest creatures? Experimentation is needed.

The pet robot should taste "right," not metallic and not like paint. We know that small children will lick the thing once in a while and the taste should be neither attractive, nor offensive, though maybe faintly salty. You don't want a child nor dog to be slurping the thing constantly. Children are discouraged from licking the cat and reverse.

In this day of high-quality audio systems, the pet robot's sonic range and style could be controllable.

The pet robot should "feel right," probably warm and soft, not necessarily furry, 98.6°F would be a sensible internal temperature with an appropriately corresponding skin temperature.

People also like to know which way is up on their pets. For protective reasons, animals are light underneath so things looking up under them mistake them for the sky, and dark on top, so that things looking down mistake them for the ground. The arrangement of colors varies, but among mammals, earthy tones predominate. Vivid reds and blues are uncommon. The combination of color and shape should reveal to small child and parent alike just where the "strong back" of the pet is. Obviously, small children will try to ride the pet robot, as they always try to ride dogs and cats. The dogs and cats ordinarily resist this pleasantry by squirming away or growling. The robot need not squirm away, but people who disapprove of seeing kids sitting on the stomach of the dog will want to be assured that they are not sitting on the stomach of the pet robot.

Just as important, the pet robot must *sound* right. Strident, systematic sounds are unsettling. Threatening creatures throughout man's long history have always made purposeful, non-random sounds and our ancestors, the people who survived stalking sabre-toothed cats long enough to have children, learned to spring to alertness when non-random sounds occurred. Babbling brooks, splashing surf, the wind in the branches, are relaxing: footfalls and cyclic sounds are unnerving. The pet robot should sound random, purring, chortling, when it is not doing anything significant, and quietly systematic when it is doing something.

If the pet robot is trundling down the hall after you, it should let you know it's there. It presumably has no claws to make a sound on the floor, as the dog does, but maybe it can make a jolly soft clicking noise of self-importance while moving, so you won't stumble over it or be taken by surprise. In this day of high-quality audio systems, the pet robot's sonic range and style could be outstandingly controllable.

Appearance, aroma, flavor, warmth, orientation and sound are all significant factors in the pet robot. Presumably, some of these factors are variables to be altered by the pet robot's environment. Considering behavior, what might the pet robot do?

The household pet is much admired when he curls up in the sun and goes to sleep. A sleeping pet doesn't look dead, nor lifeless. He looks like a live sleeping mammal. He breathes, snores, chuckles, twitches a bit, and shifts his position occasionally, often following a moving sunbeam across the floor

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as the earth turns. It should be no problem to design the pet robot to do these things in the same, reassuring fashion.

People learned many thousands of years ago that when the family meathound hears something interesting, even when he's asleep, his ears stand up. Many men have been warned of danger by the alert ear responses of a sleeping pet. Should the sleeping pet robot be less alert?

The pet robot could even control secondary home safety systems, could switch on lights or trip silent alarms.

Indeed, since the brain seems to be designed to wake up when something non-random occurs and we have considered behavior in the robot that affects that human characteristic, can we not put the same characteristics in the pet robot? Shouldn't it awaken when something non-random occurs around him? There are many different levels of activity in our ordinary environment that we learn to judge by experience. A hubbub of playing children may not disturb us, while the very subdued sound of something breaking or tearing may instantly attract our full attention right in the middle of all the fuss. We have, built-in, certain kinds of priorities. Why not build such priorities into the pet robot?

His clock may tell him, for example, that he should be quiet at night, again, not dead, but quiet. However, if non-random activity breaks out in the house, he should "investigate" that is, he should go where the action is. That's what pets are expected to do.

A pet must show interest in his master's activities and be a cheerful pal. The dog always gets up and goes to the kid who cries in the night, to the grandmother who is more restless and uneasy than usual—making non - random signals.

When there's a new baby in a household, one of the more endearing things an older, but still very young, child does is to listen very closely to what the baby is doing and then report vigorously when the baby cries. It's conventional for a little kid to run through the house, saying: "The baby is crying, Mom, the baby is crying," when Mom already knows. Why not the pet robot?

Different households have different needs, but people with small children are always pleased to see the family dog or cat hovering protectively and kindly around the fry.

Notice that babies are commonly surrounded by a mild aroma of sour milk. How difficult is it to build a sour-milk detector into the pet robot so that it constantly seeks the baby? Some override will prevent the pet from climbing on the kid, but the robot will hang around the baby, sleeping, listening, shuffling about. Then, when the baby cries, the pet robot may run through the house (at no more than 2 mph) saying in a charming little voice: "The baby is crying, someone come, the baby is crying." Is sour milk an inadequate lure? Surely the baby may be sought by other means.

It's entirely possible the pet robot can learn to identify members of its own family (inexpensive enzymatic sensors might serve) and to be ill-at-ease with strangers—until he is taught that some of them are friends.

Imagine that you are a burglar. You have entered an apparently unattended house and are rummaging around for the cameras when something you can't quite identify hastens into the room to announce in a slightly hysterical voice: "I think it's only fair to warn you that there are rattlesnakes loose in here!" Then the thing groans miserably and loudly and settles down to follow your moves with its sensors. From time to time, a rattlesnake rattle is heard in the room, accompanied by little gasps. This might inhibit you from reaching into dark corners.

Of course, the pet robot might have a considerable repertoire of such activities, designed to speed the parting guest. It might even control secondary systems that make sounds, switch on lights or trip silent alarms in some random and unpleasant fashion. No violence. No threat of violence, merely uncertainty.

When the pet robot is not trying to be menacing, it may even

try to be very friendly. When a dog pants and lets his tongue loll out, especially while wagging his tail, people take a shine to the cheerful beast and reach out to scratch his ears or pet him. This arises from tens of thousands of years of observation that a dog is this configuration is not tensed up to bite somebody and that's a relief in itself. Can the pet robot give such signals? Of course.

The pet robot should come when he's called, no great technical problem now. He should go when somebody says "Go!" stop when sombody says "Stay!" He should learn not to cross a barrier, so that he can be fenced into some area.

The pet robot will be acceptable if it does things that are appropriate to changing situations, but not entirely predictable. The behavior of a household pet is predictable *in general*, but not in detail. It is slightly random, surprising, revealing of the personality of the pet.

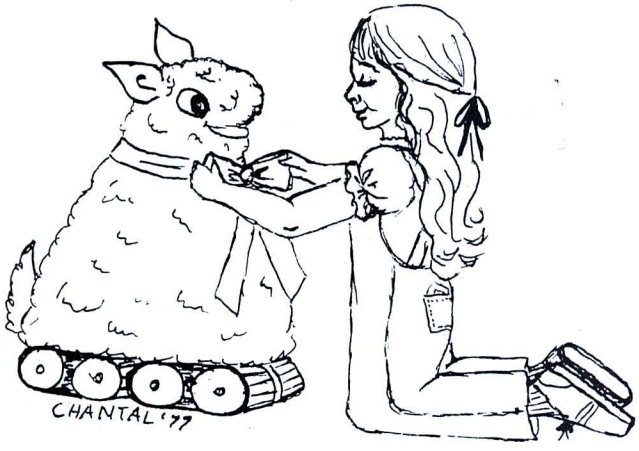
It is out of context here to speak of useful tasks the pet robot might perform—fire alarm, intrusion alarm, small tool carrier, paper fetching—until the pet-like characteristics that allow the creature to be loved are established. People do grow fond of machines. People become sentimentally attached to *old* cars whose increasingly random performance they have come to know. They gloat over, but they are not *fond of* new cars.

Pets have one more characteristic: they depend upon their masters for care. No animal that hunts the countryside for his own food, who slinks away into a dark hole to care for his own hurts, is considered a *pet*. An independent animal of that sort may be an acquaintance, even sort of a friend, but he is not a pet. History suggests too strongly that a noble, independent, proud creature is dangerous, not to be trifled with, certainly not to be left with the baby, whom he may come to regard as a possibility for lunch.

Let the pet robot cry when it is hurt and come to Mom for aid. Let it grow more alert toward dinner-time, then more active, then positively importuning, softly whining and eager. Let the pet robot respond delightedly to the sound of the dinner bell, snorting deliriously when his battery charger is plugged in by the loving human hands.

No characteristic of pets discussed here (surely others have been omitted that are worth discussion) calls for any sort of technical breakthrough. All of this is within present technical capabilities, within reasonable cost constraints.

The problem is not to make robots do something novel, but to let them do things that are familiar and welcome.



Footnote.

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ROBOTICS SECTION

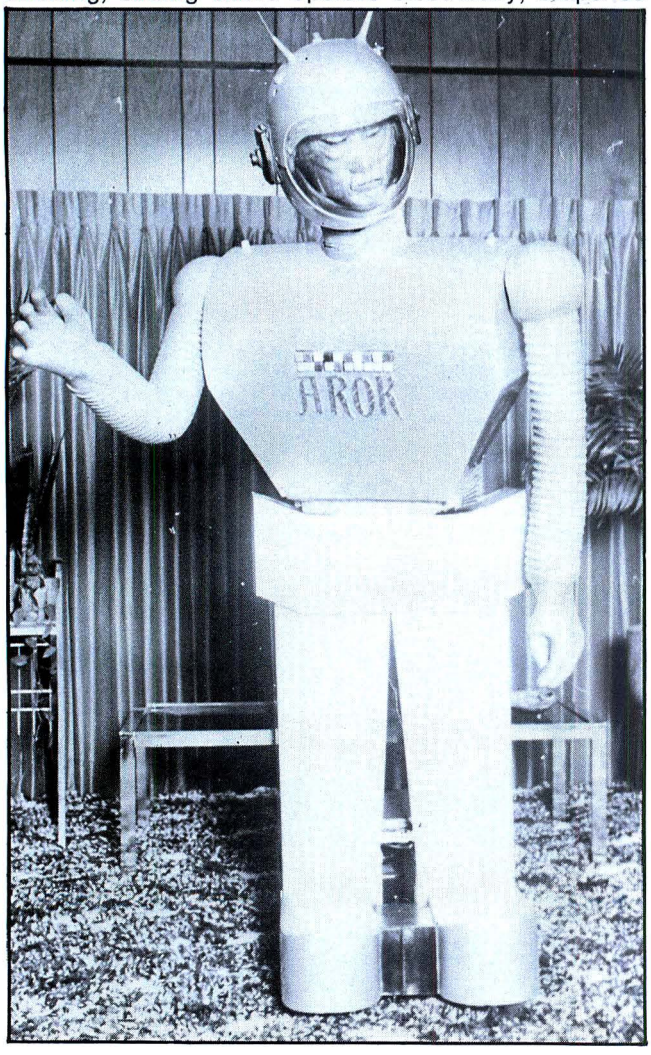
AROK

By Linda Folkard-Stengel

Inventor Benjamin Skora is a resident of the Chicago area, a region notoroius for its fearsome winter climates. Back in 1949, Mr. Skora designed a system into his car that would enable him to start the motor of his car and warm up the passenger cabin before the driver had left the warmth of his home. He operated this convenient device for many months. Its success inspired him to add to the unit until he had designed a system by which the driver could sit on the porch and direct the car to start, stop, open and close the windows, honk the horn and wipe the windshields.

With each new car Mr. Skora acquired, he built in his telemetered system with improvements. The remote-controlled car became a local attraction and soon the inventor was displaying his system for promotional purposes.

What could so successfully be done with a motorcar, might also be done for an indoor machine. When the Skora family built a home in Palos Hills; Illinois, Ben Skora incorporated many futuristic features into the dwelling; sliding doors operate electrically, draperies open and close by push-button and a revolving turntable contains a seating arrangement which swings around to open to the patio in good weather. Kitchens and bathrooms are automated for maximum convenience. All that was needed was a robot to push the buttons—and Ben Skora designed one.



AROK—

The name AROK is derived from "Skora" eliminating the "S" and backwards. According to its creator, it is more than a mirror-reversed version of the designer; it is a crystallization of the upwelling vapours from the wellsprings of creativity resting quiescent within the human consciousness. Ben Skora has no training in electronics; a former owner of a recording studio, he is completely self-taught.

AROK has an insurable value of over a million dollars. It is 6'8" tall and weighs 275 lbs. It has the capacity of lifting 150 lbs. Power is derived from two 12V car batteries, one to supply power to the electronics and the other to the drive motors.

FRAMEWORK

The frame at the base is made of heavy angle iron. The entire upper frame is aluminum. The batteries are placed on platforms in the feet and the drive mechanism in the base. This gives the unit a low center of gravity, enabling it to bend over and lift weights without tipping over. He can bend at the waist to a 45% angle and turn the upper torso to the right and left.

The integument of the body is aluminum sheeting, hand formed and welded.

The "skull" is molded from fibreglas and the face shield is from a motorcycle helmet. The face inside the helmet is a rubber mask which covers the actuating mechanism for the jaws.

The flexible neck enables the head to move forward, backward, right and left. This movement greatly enhances the lifelike appearance, especially during conversation. The electromechanical jaw actuators contain attachments to the inside of the mask at the mouth. A microphone and a speaker are contained in the head. As the operator talks into the microphone in the control panel, the robot jaw mechanism responds to the voice causing the lips to move.

The arms are jointed at shoulder, elbow and wrist. The arms can raise from the shoulders, the elbows can bend.

The rubber-glove-clad hands are designed on bushings and screwjacks which allow for grasp, roll and rock motion creating an uncanny illusion of humanlike motion.

AMBULATION

AROK moves at a variable speed from two to three mph, forward and backward on wheels with a turning radius equivalent to his own length. The wheels are set

into the bootshaped housing for the batteries. Control of ambulation is achieved by telemetry and built-in program.

TELEMETRY

Three antennae in the head receive and transmit signals from the control panel through F.M. wavelengths. The tones are generated by conventional telephone pads The control panel has a bank of buttons, each representing a field of function and corresponding to a motion function on either side of the robot. To raise the right arm, Button #1 is depressed; to lower the right arm, #2 Button is actuated; Button #3 raises the elbow up and #4 lowers it. The control pannel supplies the robot with 36 functions at present and an additional 36 functions are planned to be added in the near future.

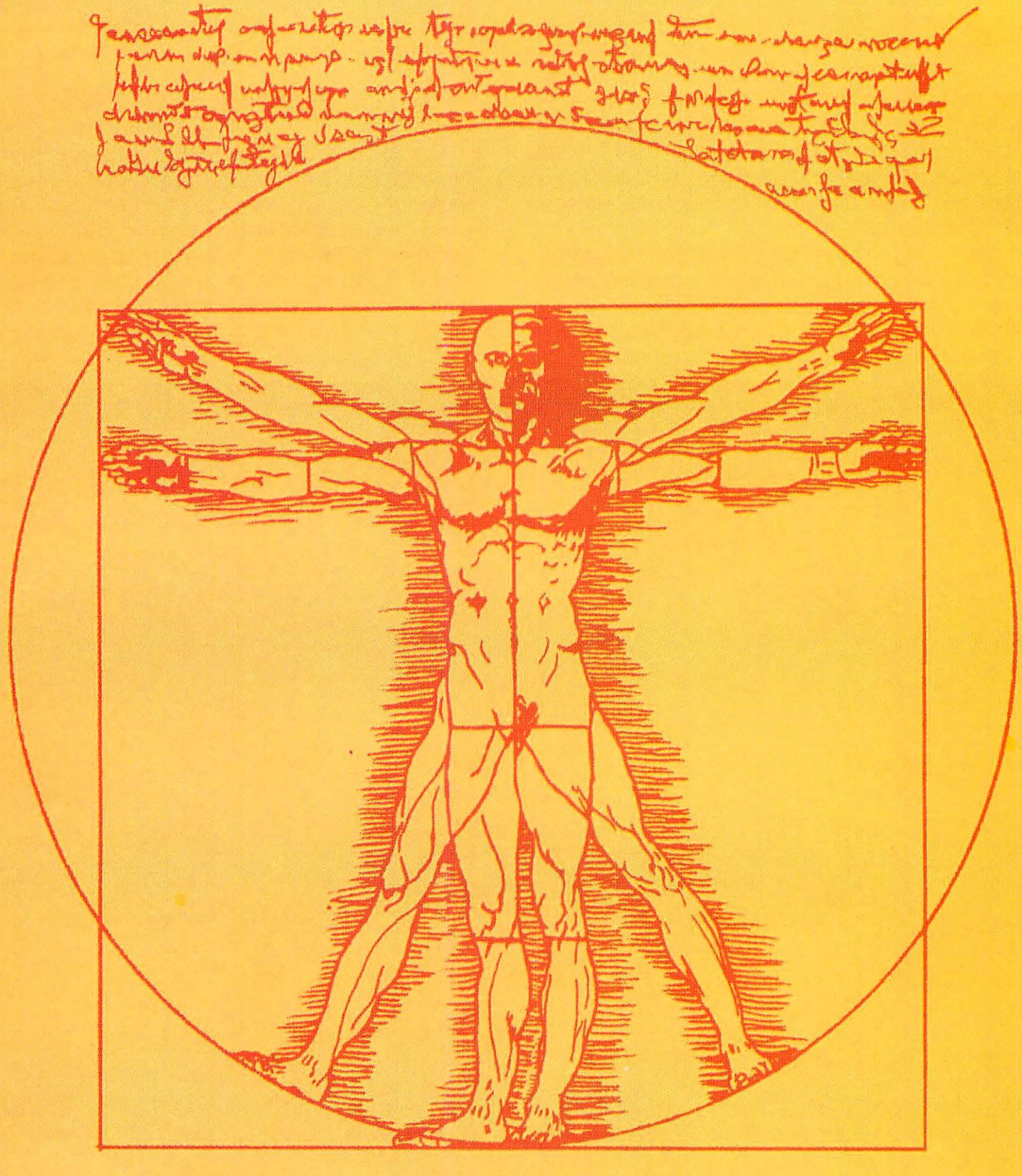
Signals transmitted to the robot are filtered through a set of active filters then to relays for two-speed modulation of the motors in the various areas of the body. There are a total of 15 motors, all of them redesigned automobile electric motors connected to approximately 35 relays and hundreds of solid-state ICs and transistors.

AUTO-OPERATION

A memory tape enables the recording and programming of the telemetered routine to be repeated at will. Ben Skora at present is working on autonomous movement by means of the microprocessor. His programming routines will be the subject of future articles.

PRACTICAL APPLICATIONS

The Skora robot at this time vacuums the carpet, walks the dog, picks up and carries parcels, serves drinks and answers the door. Its principle function at this time, however, is a demonstration device and a public relations spokesman for the coming age of cybernetics. Children find the adult-sized toy irresistible and knowledgeable adults listen attentively as Ben Skora describes his future plans for a bio-feedback organism operated by alpha waves.



The Romotoid/Android Project

written by Roger Charles Garrett

THE REMOTOID/ANDROID PROJECT

By Roger Garrett, President
Rhode Island Computer Hobbyist Club

For the past seven years I have been privileged with the opportunity of working with the Robotics and Artificial Intelligence Research Association as Director of their Applications Design Center. This report is meant to give an overview of what has been done here since the organization began back in June of 1978 and particularly since I joined them in August of that year. I had been working independently on robotics theory in a small laboratory of my own when I was asked to join the Association. The work that we have accomplished can be logically viewed in three phases, and I will discuss them in that manner.

PHASE 1

The first devices we built were quite crude. The intelligence of these mini-robots was about on the level of a smart caterpillar. They were simply mobile devices, usually not more than one or two feet high, employing a variety of manipulative devices, including the common claw used frequently at that time by amputees. Of course ours was under computer control and often linked to a visual input device so that the robot could keep track of its motions by watching itself.

Many such devices had been used in control applications where the function was a simple one. One of the first uses was in auto manufacturing where the robot did the tedious manual labor of spot-welding certain parts on the door frame. The robot had enough intelligence to recognize poor welds, misplaced parts, and would notify the maintenance crew if it ran out of oxy-acetylene.

This was the general trend of our first phase of research. It was basically a learning experience for most of us on the project. We were re-hashing much of the work that had already been done in order to gain insight into the basic theories and design problems of robotics. Phase 1 lasted about seven months since the corporation funding our work was getting anxious for more advanced development and we were "encouraged" to proceed to our next phase.

PHASE 2

We were finally getting into an atmosphere of true research. We first defined a simple outline of the direction we hoped to pursue. The concept we had envisioned was a completely mobile machine, fully under human control but capable of independent intelligence in compliance with the Three Laws of Robotics, having all human as well as certain extra-human senses. We obviously had undertaken a huge task.

The *real*, understandably, was to be somewhat less than the ideal, limited as we were by the technologies of the day. A major breakthrough would be required in the field of artificial intelligence along with cheap mass memory and super high processor speed in order to implement the independent "mind" of the remotoid (**REMO**tely-controlled and**roid**). We ended with what was a developmental stage device that would serve as a starting point to the future of robotics.

Basically we developed a remotoid controlled, not by artificial intelligence (although intelligent I/O and some intelligent processing was utilized), rather by a human operator. The remotoid was built using the human body as the model. The senses of sight, hearing, and touch were included. Mobility was achieved using a recently developed artificial muscle. The remotoid was, in effect, a remote I/O device to the operator's senses.

The concept we envisioned was a completely mobile machine in compliance with the Three Laws of Robotics. That would require a major breakthrough in the field of artificial intelligence.

A suit, similar in appearance to a scuba diver's wet suit and suspended from a harness similar to that used by NASA to train astronauts was worn by the operator. The operator was suspended in the harness, allowing him all degrees of freedom. Every movement of the operator was duplicated by the remotoid, every force exerted upon or sensory input experienced by the remotoid was duplicated for the operator. The effect to the operator was as if he "occupied" the remotoid, and as if he were experiencing what the remotoid experienced.

A device similar to this had already been tested in independent research done by others in the early 1960's but with much less sophistication. A helmet had been fitted with Binocular CRT's so that the person wearing it could be presented with three dimensional computer-generated images. The helmet was attached by means of a moveable arm to the center of a work area giving the operator free mobility within the laboratory. The computer could detect the position of the helmet—and hence the operator—in relationship to the center of a room by means of sensors attached at the fulcrum points (elbows) of the arm. The computer displayed images to the user as line drawings. What the user saw was an apparent three dimensional "object". Since the computer knew the user's position at all times, as the user moved about the room the computer displayed different perspectives of the displayed object. The effect to the user was that he was walking around, and even through, the visualized object. This original experiment had provided the incentive for much of our own work.

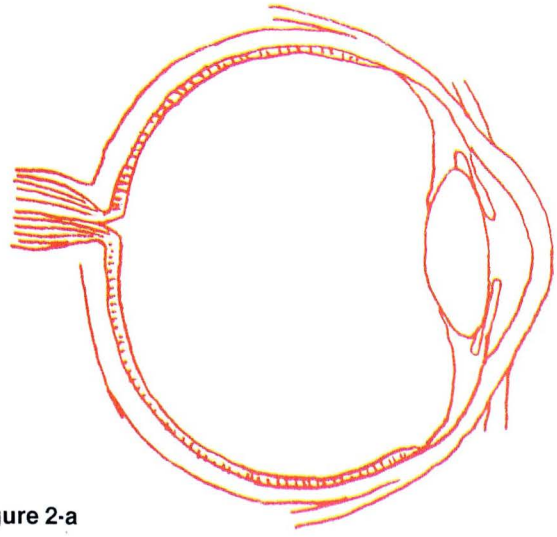
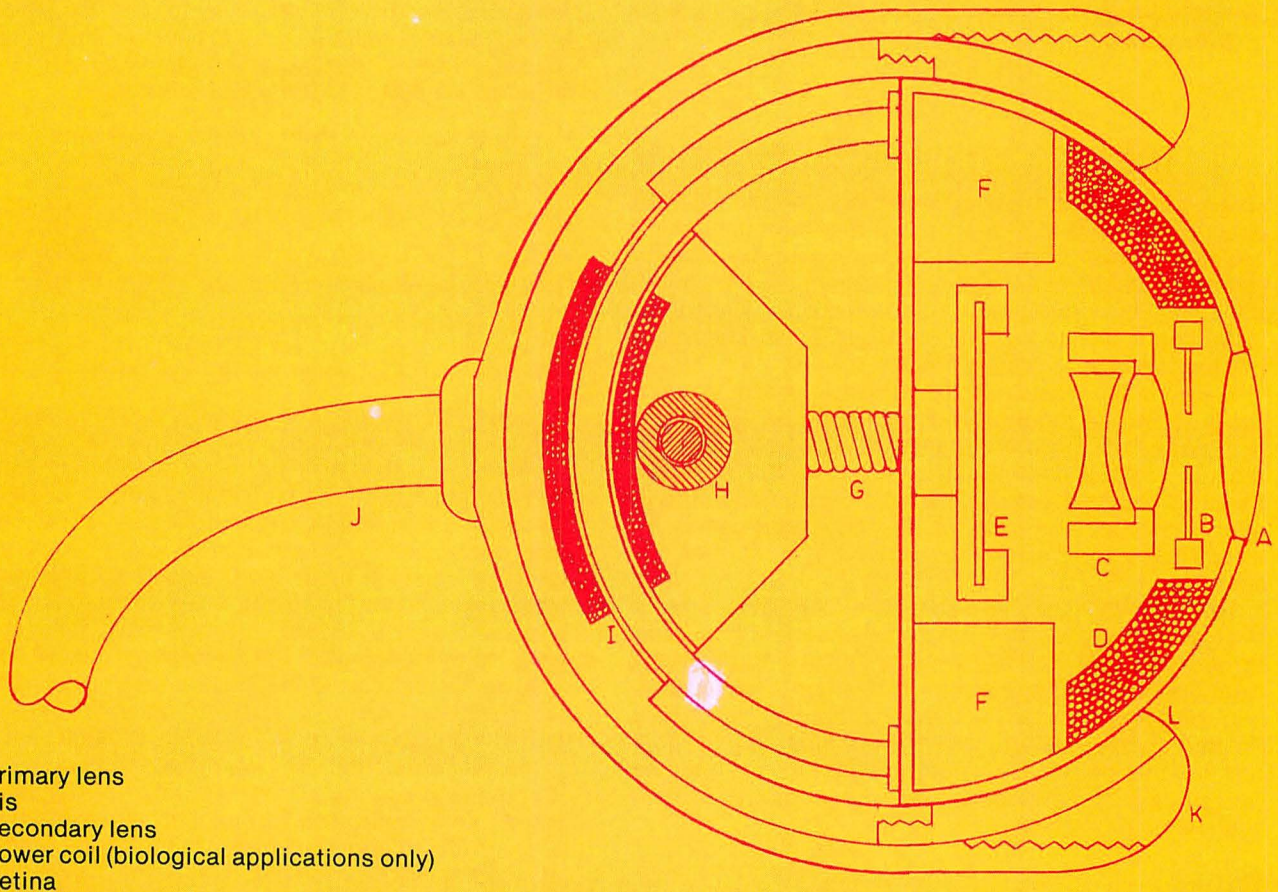


Figure 2-a



A. Primary lens
B. Iris
C. Secondary lens
D. Power coil (biological applications only)
E. Retina
F. Driver logic circuitry
G. Internal transmission trunk
H. Horizontal positioning shaft
I. Vertical positioning shaft
J. External transmission trunk
K. Secondary casing
L. Primary casing

Figure 2-b

THE BARE BONES

The skeletal system was produced using a process which emulates the effects of petrification. In the normal process the living tissue of a plant or animal is replaced, over a very long period of time, by the minerals in its environment. The artificially induced petrification process takes only one week for small samples of 4 ounces or less. For the remotoid, a human skeleton was obtained which met the physical characteristics necessary to contain all of the other hardware. The bones were separated and the petrification process applied, using an alloy of aluminum as the replacing mineral. The process of petrification preserves all the structural characteristics of the original bone. Using aluminum provided us with a skeleton which was well within the weight limitations yet which exhibited high structural integrity. The completed remotoid is able to withstand pressures as high as thirteen atmospheres and accelerations up to 4.2 g. The acceleration limitation is more a function of internal hardware designs rather than of the skeletal system. (See Figures 1a and 1b.)

VISUAL SYSTEM

The visual system, like most other parts of the remotoid, emulated the human body, (Figures 2a and 2b). It was a stereo vision system and sensitive to a variety of wavelengths of light, had independent motion control over each "eye", and had a large depth range. The physical shape of the "eye" was identical to the human eye. It resided inside an aluminum socket using nylon as the lubricant seal. The optic nerve was a parallel I/O channel, accepting as input a variety of instructions and outputting the intensities and spectral information of the individual "cells" of the retina. The retina is a light sensitive 1024 x 1024 element matrix giving a resolution approximately twice that of standard American television. The user could, under software control, select any of a variety of spectral sensitivities, making him capable of seeing in the dark, for instance, by switching to the infra-red sensor array.

The separate light sensor arrays were interlayed on one chip. When a new array was chosen it would also bring in the corresponding lens system, since different wavelengths refract differently. The lens system was under operator control and provided telescopic as well as microscopic vision. In this way the eye need not have the resolution of the human eye since the remotoid could "zero in" on areas of its field of vision to discern a higher degree of resolution than normally available at a wide-angle setting.

I should point out that a modified version of this "eye" has been accepted for preliminary medical testing by the Association of the Blind in Sweden. We are aiding them in the development of a direct intra-neutral link to allow connection with the optic nerve. This is still in the developmental stage and we cannot say at this time what are the chances for success although several laboratory test animals have been attached to it, and the results are encouraging.

The operator's end of the visual system was a binocular solid-state display system similar to the one used in the early 1960's. Our setup gives color as well as sophisticated depth perception. It was built into the head gear of the operator but did not interfere with his normal motions for it was comparable in size to a pair of well-fitted prescription glasses.

TACTILE SYSTEM

The tactile system (feeling) used a material which increases electrical resistance as pressure is applied. The

Figure 1-a

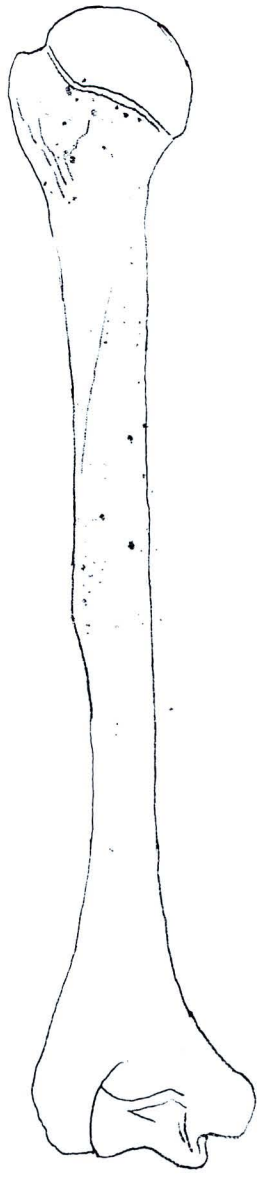


Figure 1-b

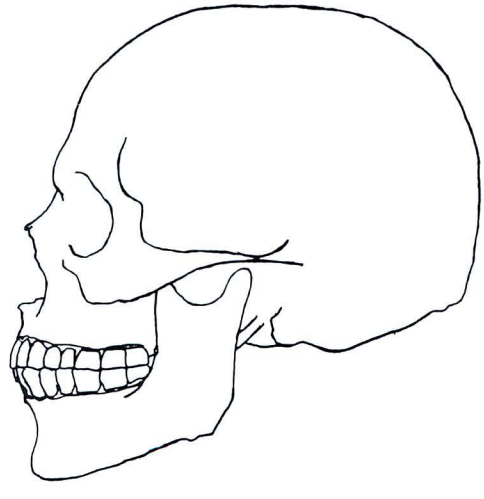
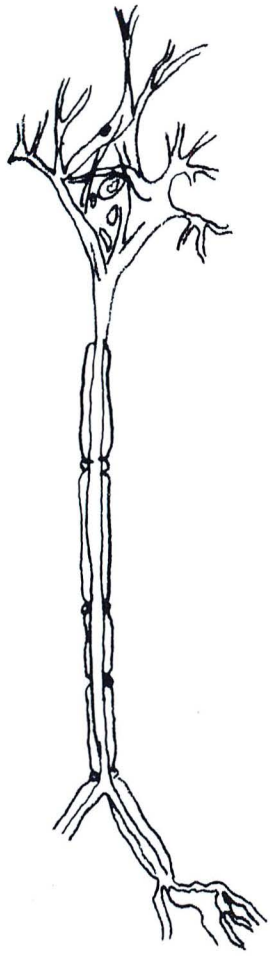


Figure 3



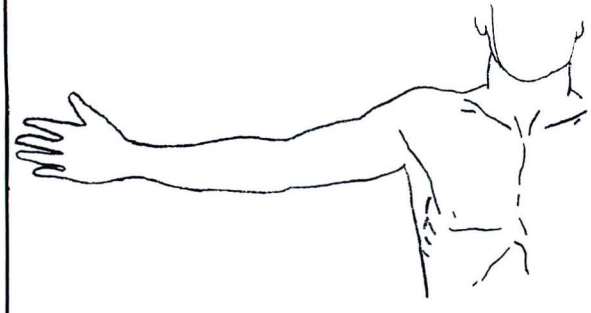


Figure 4-a

remotoid was covered by a thin matrix of this material which looks somewhat like a quilted body suit. Each square centimeter of the remotoid's surface was addressable by the tactile system micro-processor. In particularly sensitive aras such as the hands the matrix were further divided into square milimeter sections, (Figures 3 and 4-a and b.)

The operator wore a suit which provided to him the tactile experiences of the remotoid. It accomplished this by means of a matrix network of hydraulic reservoirs. When the remotoid "felt" something i.e., encountered a force applied to its skin, a fluid would be forced into the corresponding reservoir within the operator's suit which applied a measured amount of pressure to his skin. While it did not provide full tactile sensations the reservoir system was sufficient for most applications. In some situations even roughness could be felt, although the operator required at least 15 hours' experience.

A temperature sensing system was included and was tied in with the tactile system. At each matrix point of the tactile matrix there was a heat sensor on the remotoid and a heat pad on the operator.

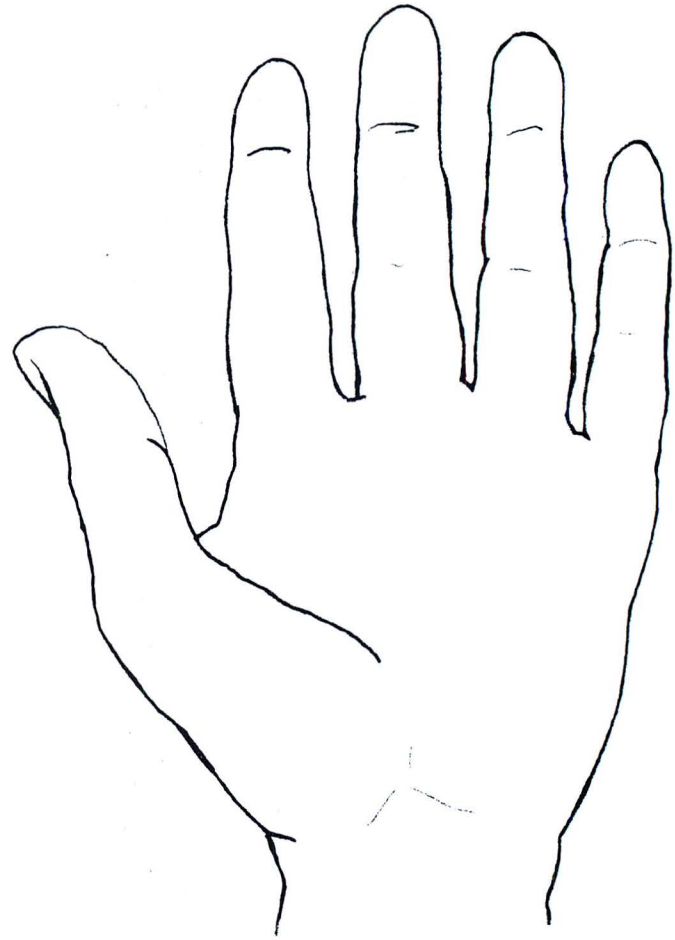


Figure 4-b

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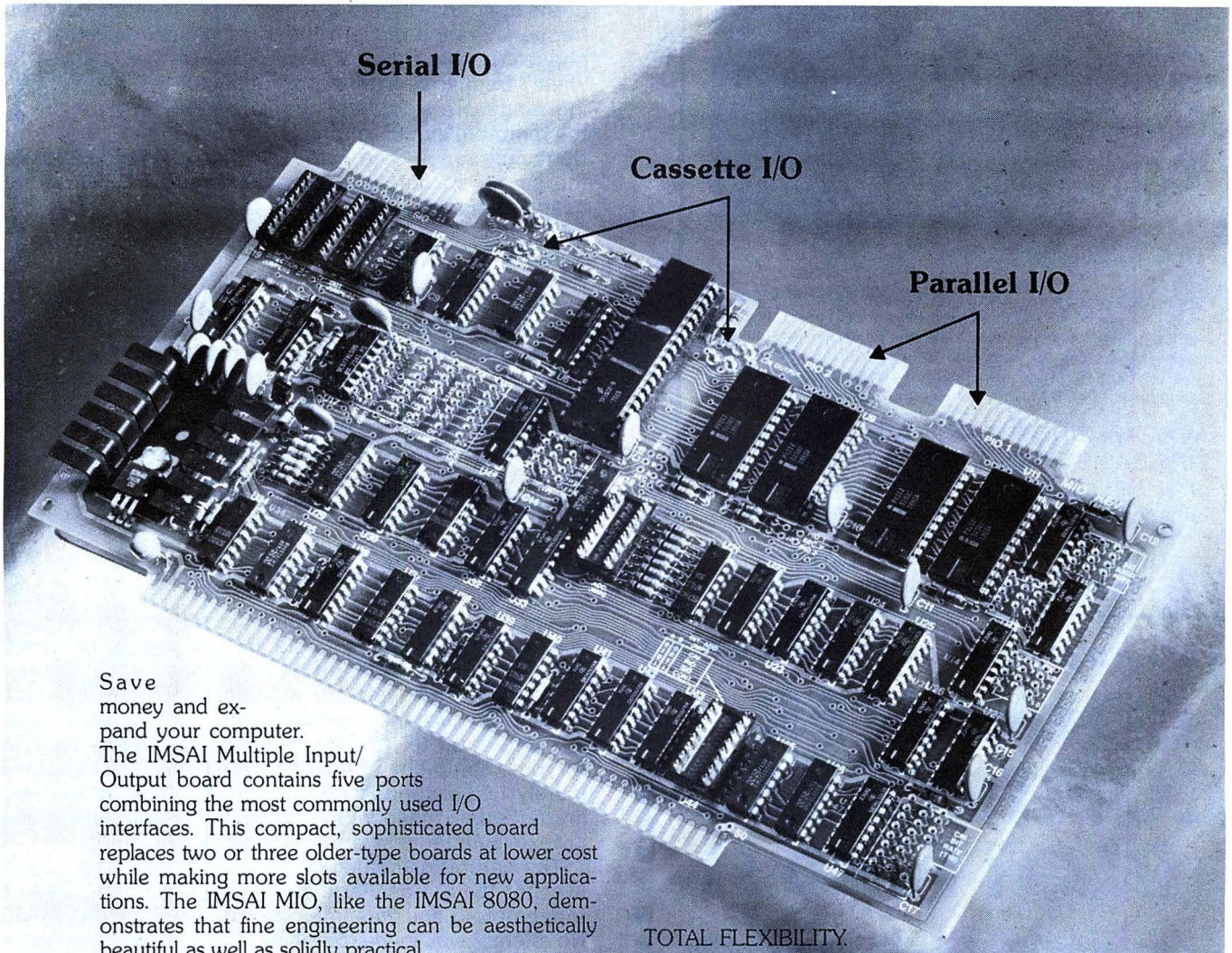

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AURAL SYSTEM

The aural (audio) system was probably the easiest to implement. It was simply a pair of highly sensitive frequency-tunable microphones in the "head" of the remotoid and a pair of high response earphones for the operator. The earphones were a special set made for this purpose and were much smaller than conventional earphones, fitting almost completely within the aural canal of the operator, (Figure 5). The operator could select the frequency range of both the microphones and the earphones. In this way it was possible for the operator to "hear" frequencies normally outside of the human hearing range. He would set the earphones to *normal* and the remotoid's microphones to the selected "inaudible" frequency range. The aural software then would scale the sound so that the operator received it within his hearing range.

VOCAL SYSTEM

Another simple system was the vocal output. In some situations the remotoid would require the ability to converse with other beings in their natural language. This was accomplished with a microphone in the head gear of the operator and a speaker in the remotoid. It was felt that it was not necessary, at least at this stage of development, to have the remotoid actually "talk" by mouth/larynx/voice box interaction so a speaker replaced the section of the remotoid's head where the mouth would normally be, (Figure 6).

ATMOSPHERIC SENSORS

Since the remotoid was planned for environments in which the atmosphere might be dangerous, or where certain information might be determined about the environment by analysis of the atmosphere, a device was developed which takes samples from the atmosphere and analyzes it as to its constituent parts. The cycle time for one complete atmosphere analysis was approximately 1.03 seconds with some portions of the analysis (in particular those which detect extremely dangerous or toxic substances) requiring only .005 seconds.

The natural placement for the input port and output vent for the atmospheric system was the nose area of the remotoid and was implemented as such, (Figure 6). No attempt was made to transfer the sensual information to the operator's nasal senses. Information about the atmosphere was available to the operator via aural data from the main control computer or by visual data superimposed over his field of vision.

MUSCULAR SYSTEM

This system probably caused the most problems in implementation. Indeed, if not for the timely development of the artificial muscle by E.T. Klaffen of M.I.T., the remotoid project would have ended at this point.

Dr. Klaffen was successful in isolating the bio-chemical structure, triszatin, responsible for natural muscular movement[1]. By coupling the bio-compound with the plastic Pheda-toluel[2], he was able to preserve the flexibility and responsiveness of natural muscular movement. By itself, triszatin requires a constant supply of nutrients, via the blood, to stay active, and the presence of a separate chemical compound, thoran-bi-toxylate in order to trigger the contraction reflex. Dr. Klaffen was able to

1. See *Artificial Muscle* by E. Klaffen, pp. 29-32 *Biomedical Research Journal*; January 1978.
2. Pheda-toluel is the trademark of the pseudo-plastifier compound developed by 3M Corporation in 1978.

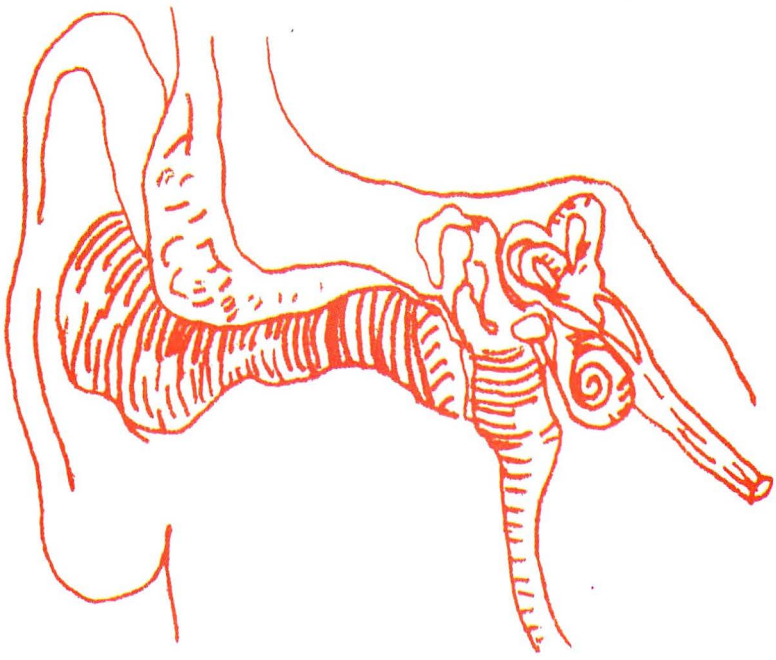

Figure 5

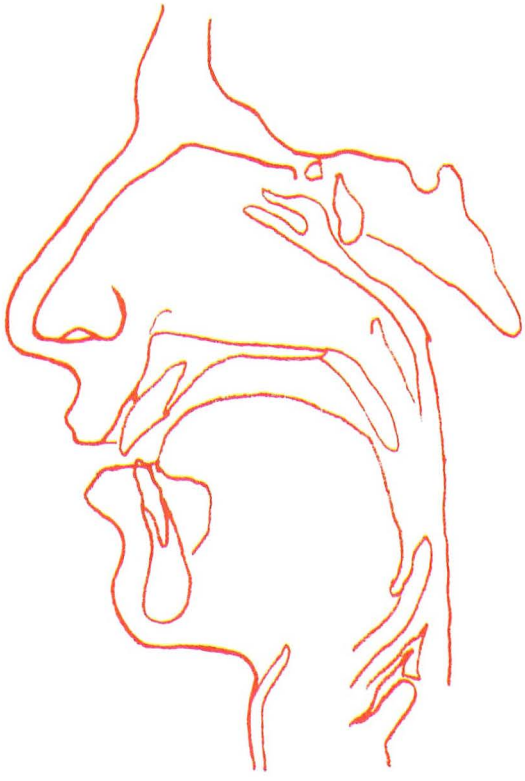

Figure 6

alter the structure so that only a small electrical charge was required to induce the reflex. The Pheda-toluel, in effect, acts as a catalyst and keeps the main compound, triszatin, "alive".

The artificial muscle was easily formed into any required shape and its linear molecular structure provided complete control over force vectoring. The muscles were then attached to the skeletal system in the manner of a cadaver were being restored after a major autopsy. A "muscle addressing" scheme was devised to enable the muscular system microprocessor to control all movement, (Figure 7.) An added advantage of the artificial muscle was that it provided its own feedback. The microprocessor could easily determine the position of any part of the remotoid or force being applied to it by "reading back" the resistance factor from each muscle.

COMMUNICATIONS SYSTEM

A powerful radio communications link was set up between the remotoid and the operations station so that it could be used at great distances from the station. The use of a satellite relay system was considered at one point during development in order to allow global operations, but was found to be impractical because of the size and weight of the receiver/transmitter. Perhaps a back-pack similar to the PLSS (portable life support system) used by the Apollo astronauts would make this mode of operation possible in the future.

Power Supply

We were fortunate in not having to rely upon simple rechargeable batteries or fuel cells for the power source. We had received permission from the Atomic Energy Commission (INTERNERG) to test their recently developed atomic energy cell. While that may sound like something from a 1950's Japanese science fiction movie the concept is quite simple.

Many semiconductor materials are sensitive to light and other forms of radiation. It is that feature that enabled the development of photo-transistors. A similar principle is utilized in forming an atomic energy cell. (Figure 8.) Alternate layers of plutonium (or other suitable radioactive material) and a radiation sensitive semiconductor PN junction are deposited upon an inert substrate. The entire package is then coated with that same inert substrate and electrical connections made. The radiation knocks off electrons from the layers of semiconductor material in the same way that photons knock off electrons in photo-cells. The result is a self-contained power source. Enough of these tied together and we were able to supply all of the needs of the remotoid.

SAFEGUARDS

Override systems were necessary to safeguard the operator. For instance, if the remotoid being used in a dangerous situation such as deep sea diving and the remotoid itself was crushed by water pressure, it would not be in the best interest of the operator to have the same forces applied to his body. Likewise if a blinding flash of light occurred to the remotoid, the visual input to the operator should not blind him as well. The safeguards were simple, however, and easy to implement. The feedback devices on the operator were made so that they cannot—under any circumstances—exert dangerous pressures, excessive light, etc., to the operator.

For example, in designing the visual input for the operator a solid state display device was used to display the image and the maximum light output of the display was such that it was below the danger threshold. Also, movement and pressure devices on the operators

Figure 7. The development by E. T. Klaffen of MIT of the artificial muscle provided the necessary mobility for the remotoid. He had combined the biological triszatin and the artificial compound, pheda-toluel, to produce an electrically stimulated carbon chain capable of contraction.

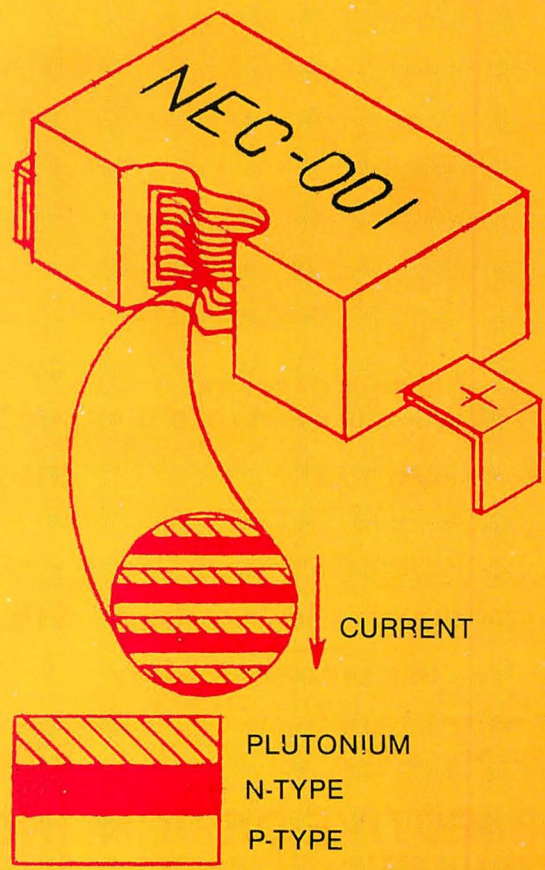

Figure 8. 'Nuclear Energy Cell—Cutaway View'.

suit were designed so that they cannot exceed certain predefined limits. These were hardware design safeguards and were easily implemented since they were well within the current technologies.

Software safeguards too, were used to protect the operator, but hardware was the main protection. Software safeguards were needed more to insure the remotoid's well being. The software was used to inhibit the operator from causing the remotoid to entire environments which would prove harmful or dangerous. In this respect the remotoid does have some intelligence of his own. An operator might want it to touch something which was too hot for the remotoid to handle. A temperature might be suitable for the operator, since he would be protected by the hardware safeguards, but if the remotoid would be endangered the software would make it impossible for the operator to force the movement of the remotoid's hand. There were of course, overrides. The operator was always in ultimate control via hardware and software override systems. Such overrides would be used, for instance, where the destruction or damage of the remotoid was necessary to accomplish some goal.

APPLICATIONS

The remotoid has been thoroughly tested and is currently being used in several applications including radioactive isotope processing at the INTERNERG installation at Houston.

The first underwater use of the remotoid was in the recovery of a minisub and its two occupants from a crevasse in the continental shelf off the New England coast. The craft had lost power at a depth of 6,000 meters and no other craft capable of that depth was immediately available. The remotoid was sent to the destroyer which had served as the mother ship for the minisub. Since the portable operator's unit had not been completed at that time, a radio link was established between the destroyer and the remotoid laboratory in New Jersey. A sonar link was established with the remotoid so that control could be maintained while it was submerged.The operator succeeded in retrieving the minisub by "swimming" the remotoid to the craft and attaching a tow line.

PHASE 3

This phase was the most rewarding and has provided us with the greatest professional satisfaction. We finally created an android[3]. This was not, however, accomplished on our own, and credit must be given to the corporations which made solid-state mass memory and the computer-in-a-Qube[4] so readily available. The Artificial Intelligence Group of our association had been doing extensive work in parallel to our work on Phase 2 and the remotoid provided them with the hardware outlet for their software systems.

The major change to the remotoid was the addition of what we call a "mind". At this point our remotoid became an android. It is comprised mainly of fifteen intelligence Qubes each containing several CPUs and 256 megabytes of NDRAM (Non-Destructive Random Access Memory, in 32-bit bytes). The Qubes contain the intelligence of the android. There are no clear-cut divisions between the intelligence centers of the Qube system. The software was written to utilize heuristic interrelational intelligence. What this means is that each portion of the software has access to and is influenced by the operations of its adjacent portions. No one section controls, for example, the operations of the android's hands, it is rather an interaction of several software modules, each defined in a real-time learning mode. In effect, the Qube software simulates very effectively the working of the human mind. Half of a human brain can be removed yet the human can learn to use the remaining half to control the entire body and with little loss of memory. The Qube system, likewise, can suffer hardware damage to more than half of its circuitry without system failure.

Obviously this means that the human operator, in the usual sense, was no longer needed and the android can operate fully on its own, although there seldom are instances where we would want it to. Many of the override systems of the original remotoid were incorporated into the android to maintain the operator's ultimate control over its actions.

So far we have received permission to test the android in only a limited number of situations. Probably our greatest thrill was having our android selected for a Mars probe landing mission by the National Aeronautics and Space Administration. We are currently making preparations for the mission by teaching, 'programming' the android with the necessary skills for performing geological and atmospheric surveys.

THE NEXT PHASE

What is the next phase of research? That has not been determined. We now face probably the greatest obstacle of all; acceptance by the general public. Our work was not generally well received, in some cases even by the scientific community. We feel that we have provided society with a tool. We believe that sufficient safeguards have been incorporated into the android to remove any danger. Certainly we would expect strict guidelines for its implementation in any business or in any situation which would impact upon the economy or stability of the nation. It is now up to society to accept or reject.

3. Android is the term used to indicate an intelligent self-willed robot in human form.
4. See the 1977 March issue of Interface Age magazine for the first known description of the Qube.

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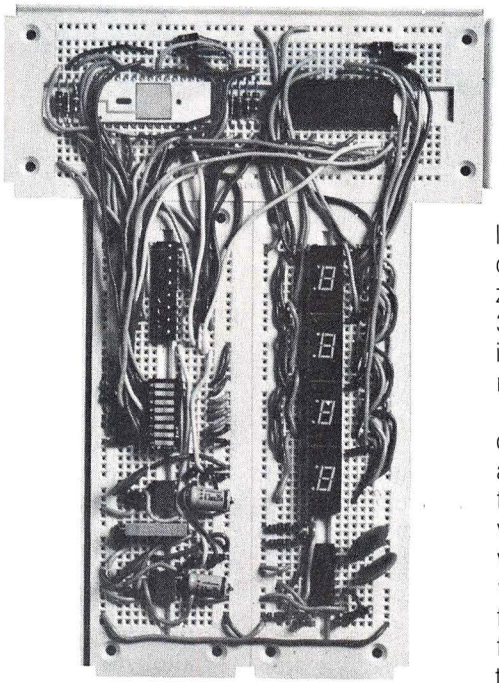

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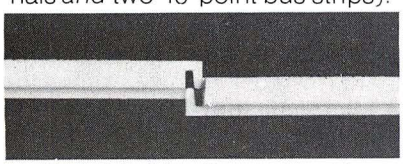

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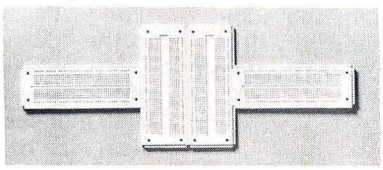

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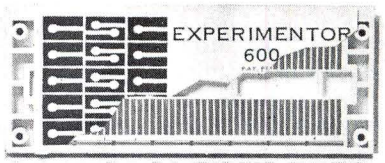

Both models feature 94 five-point terminals (vertical lines) and two 48-point bus strips (one strip shown).

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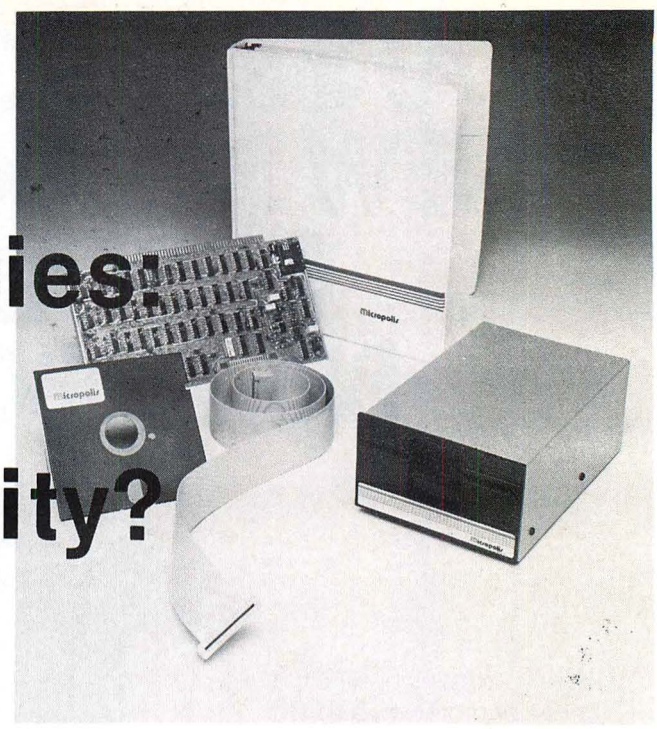
PRODUCT PREVIEW

The New Floppies: Too Little Storage Capacity?



by Stuart Mabon

BACKGROUND:—A floppy disc storage subsystem accompanied by an extended disc BASIC software package is an important enhancement to the microcomputer. Bulk on-line storage accessed directly by the software enables, first of all, fast storage and retrieval of user programs. It also allows management of data files such as inventory levels, stock and commodity trades accounts receivable, and mailing lists. The floppy disc converts an interesting toy into a powerful computer system capable of paying its own way.

PROBLEM:—The traditional implementation of file storage, using the original IBM-type 8-inch floppy disc subsystems supplied by several microcomputer manufacturers, has been fairly effective but expensive. A typical dual drive subsystem in this category still costs around $3000. Ironically, the user is faced with the prospect of connecting a $3000 "accessory" onto a $1500 microcomputer.

The older approach using the 8-inch diskettes at least had a useful data storage capacity, albeit at a high price, and successful computer usage tends to rewire increased storage capacity. Declining costs of semiconductor memory and increasing sophistication of software utilizing more main memory while at the same time allowing efficient management of large random access files, are obvious manifestations of the basic trend. The 90-kilobyte floppy disc can store an extended BASIC interpreter, a simple Disc Operating System and some application programs—that's all. This means very little room for data files. The system operates as a program loader—not a data file management system.

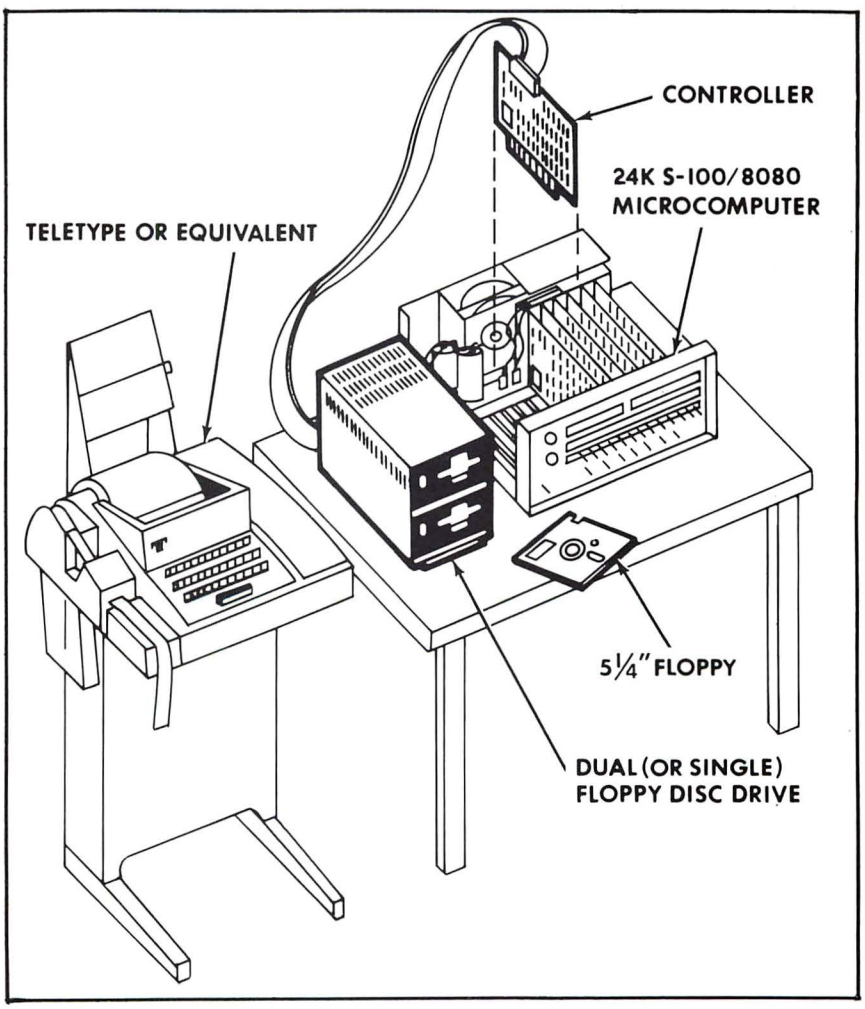
SOLUTION:—The recently introduced 5¼-inch floppy disc drive has now been integrated into a number of new floppy disc storage subsystems for use with the popular microcomputers. These new products have at least one important attribute—they are compatible in price with the mainframe. An assembled, tested, burned-in, single drive subsystem sells for around $1000. Depending on the subsystem manufacturers' ingenuity, these new random access storage subsystems range in storage capacity from 70 to 90 kilobytes. This compares with the typical 8-inch floppy drives capacity of 250 to 315 kilobytes.

A family of recently announced 5¼-inch floppy disc storage subsystems from Micropolis Corporation bridges the gap between the high-priced 8-inch and previous low-capacity 5¼-inch floppy subsystems. Single and dual drive storage models are offered. The storage capacity of a single drive model is 143 kilobytes for the MOD I version and 315 kilobytes for the MOD II version. The dual drive storage model also comes in two versions, the MOD I in which each of the two drives has a 143-kilobyte capacity and the MOD II in which each of the two drives has a 315-kilobyte capacity.

Both MOD I and MOD II drive versions utilize a 16-sector hard-sectored floppy disc, each sector containing 256 bytes. The MOD I drives use 35 tracks per surface while the MOD II drives have 77 tracks per surface. The 5¼-inch floppy discs used in the Micropolis floppy disc subsystems are identical with the one that is becoming a new industry standard. In most respects other than storage capacity, the Micropolis drive is similar to the original 5¼-inch miniature floppy disc drive, in that that double density tracking is employed a technique pioneered by I.B.M. in which twice the number of tracks per disc is provided. No increase in bit dropout rate can be observed. The exceptions are the interface connector is identical except for the addition of one or two signals designed to allow the drive to be more simply utilized in multiple drive installations. Up to four drives can be accommodated in the "daisy chain" mode (or two dual drive models). The time taken for the read/write head to be moved from one track to the adjacent one (track-to-track access time) is 30 milliseconds (instead of 40 milliseconds). The physical size of the single drive model is 3¾ inches high, 5⅞ inches wide, 12 inches deep (including power supply). The unit weighs 7 pounds. The dual drive model is 8 inches high, 9⅛ inches wide, 13½ inches deep and weighs 15 pounds. The dual drive has seven-segment drive address indicators which can be interchanged by the operator with a switch accessible from the rear, "drive selected" indicators and "file protected" indicators for each of the two drives.

The subsystems include a S-100 compatible controller


micropolis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board with an on-board bootstrap PROM removing the need for an additional PROM board or for paper tape or cassette bootstrap loaders.

BASIC:—In many respects, the most important aspect of any file storage system is the quality of the available software. BASIC has become the standard language of the personal computing world. However, there is a wide range of capabilities advertised under the BASIC name. The Micropolis uses a full extended disc BASIC delivered on a floppy disc included in the cost of the subsystem. As well as the standard BASIC capabilities it allows DIRECT commands for saving, reloading and eliminating named BASIC program files with automatic disc space allocations; PROGRAM STATEMENTS to create and delete data files and to access records within files in a sequential or random manner; and FUNCTIONS to examine and manipulate data file attributes and file space utilization. All the features are integrated into the BASIC system making it completely self contained and self sufficient.

The Micropolis system includes S-100 compatible controllers, cables and the powerful extended disc BASIC interpreter for MITS, IMSAI and Polymorphic microcomputers. The prices of the various versions of the subsystem family, range from $895 for a single 143-kilobyte, MOD I subsystem, without power supply, but with regulators which draw power from the host via the controller, to $1795 for the top of the line dual and drive subsystem with two 315-kilobyte MOD II drives, including internal power supply.

The 5¼" floppy provides microcomputer users with the capacity they need at a price that makes sense. Peripherals have always been the biggest investment in the long run for people putting their systems together—the mini or microcomputer just whets the appetite. It's the old "tail wagging the dog" story.

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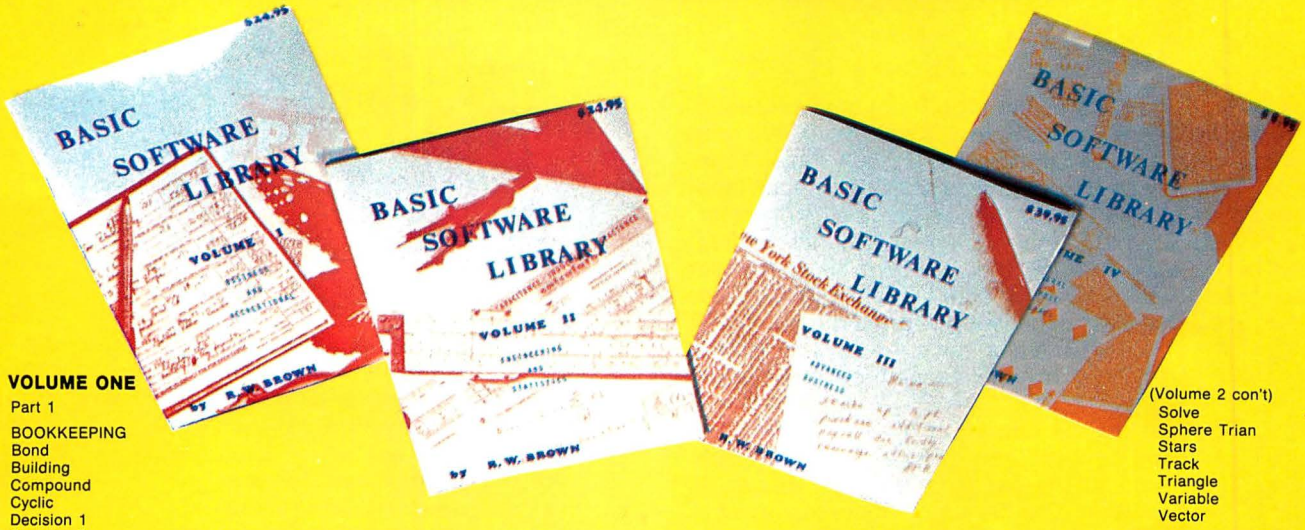

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CARD OF THE MONTH

The O P - 80 A

By Roger Edelson

This month the Card of the Month column will focus on an entire device rather than a single card. We will cover the Oliver Audio Engineering OP-80A Paper Tape Reader. This device is a manually operated paper tape reader which will read paper tape as fast as the operator can pull it through (0-5 Kcps). This exceptional reading speed is achieved through the use of a photoelectric as opposed to a mechanical sensor. The OP-80A also manages to achieve its excellent performance in a small package (4½ x 3 x 1¼) and at small cost—$74.50 for the kit version and $95.00 for the assembled and tested device.

Before discussing the operation of the OP-80A lets take a look at the circuitry and design. Figure 1 is the schematic diagram of the paper tape reader. Figure 2 provides the Parts List. The device consists mainly of a photoelectric sensor (of unnamed parentage) followed by NE555 timers used as pulse stretchers for the data signals. A single 7474 "D" Flip-Flop is used to provide a "Read Data" signal which is clocked by the leading edge of the sprocket hole. Handshaking *acknowledge* signals are also supplied to the 7474 so that no RDA signal will be provided unless a ACK (acknowledge) signal has been provided by the computer input/output interface. Additional operational signals can also be supplied by the computer to turn on LEDS—S1 and S2.

PARTS LIST

OP-80A-IC1-IC9	NE555*	$ 1.50 ea.
-IC10	SN7474	.95 ea.
-IC11	SN7437	.95 ea.
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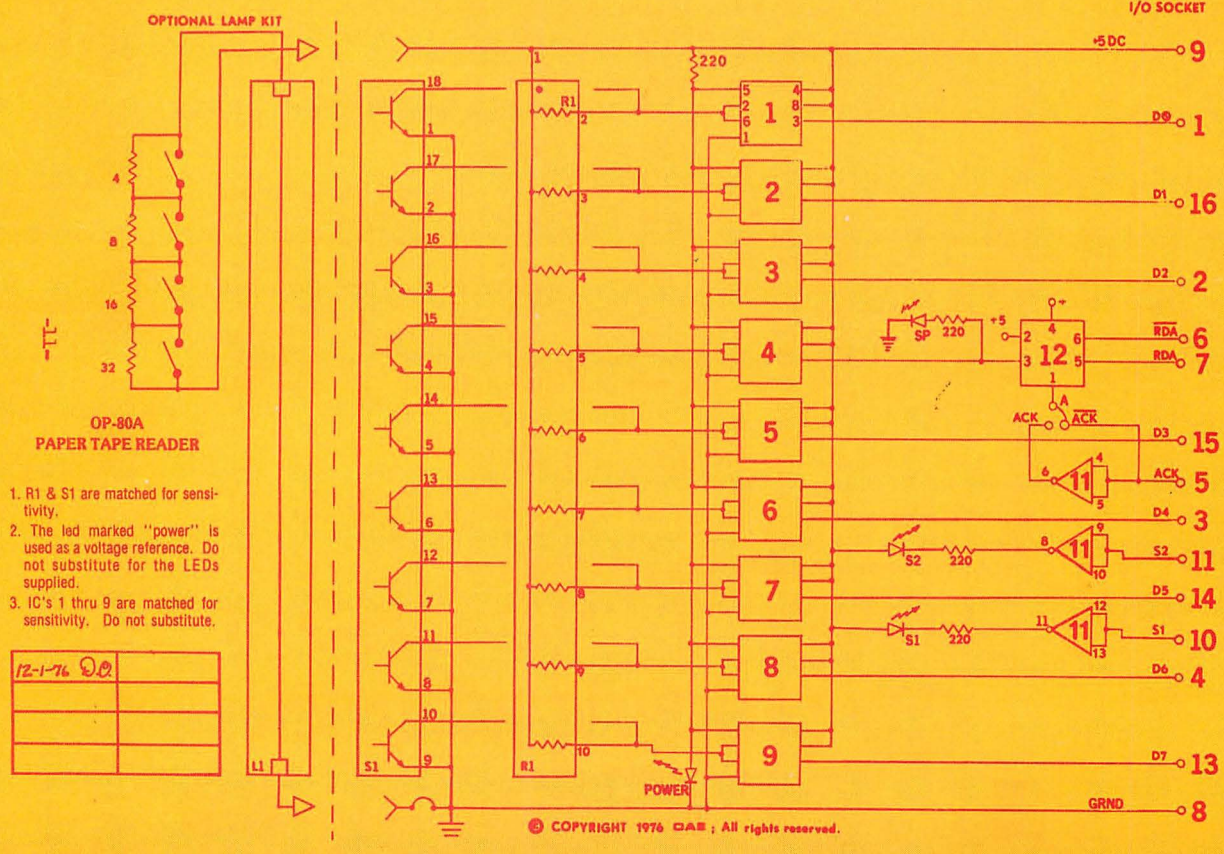
*These items are selected and matched devices. Do not order separately.

FIGURE 2



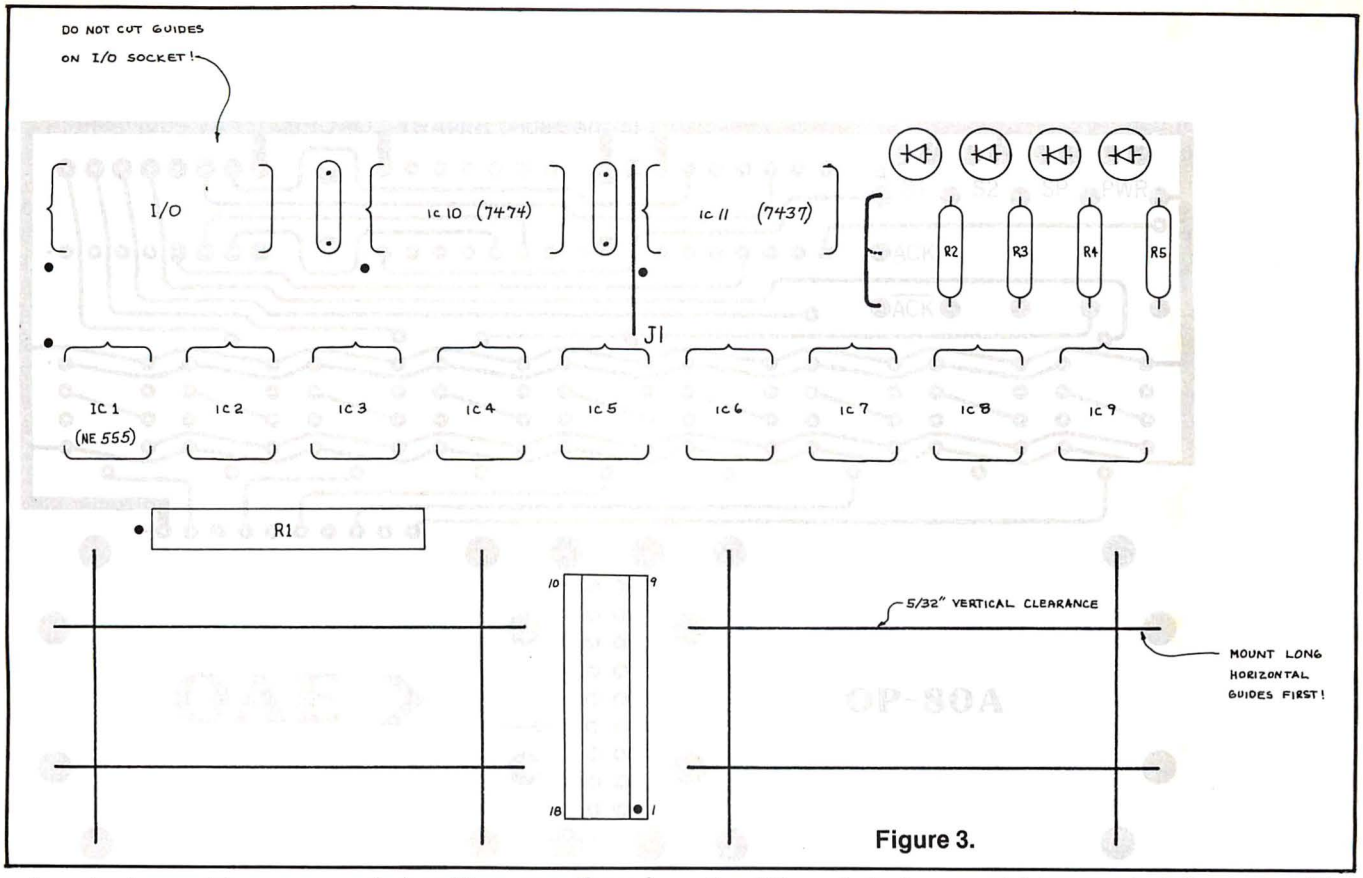


Figure 3.

In order to provide a means of signalling operation of the OP-80A a power LED and a LED indicating the sprocket hole has been provided. The power LED is also used to provide the reference voltage needed by the NE 555 one-shot timers. The schematic notes indicate that the sensor and the resistor network are matched for sensitivity as may well be required by the difficult light transmissibility problem afforded by paper tape.

Let us take a look at the kit and its assembly. The parts of the kit came well packaged and easy to identify—however, it must be remembered that there are only about 25 parts to be assembled. The Layout Diagram, Figure 3, is more than adequate, though the capacitors could have been labeled. While on the subject of labeling—OAE could have been a little more thoughtful and labeled the resistors on the schematic. It would be nice to know which one is R2, etc. Construction was straight forward and very easy though no sockets are provided. For only a couple of dollars more, OAE could have provided sockets for the IC's. When I built the unit I added sockets for the 7474 and the 7437 since they were handy. I would have liked to place socket on the whole board as I don't feel the IC's will take much removal and reinstallation.

The assembly instructions are clear and easy to follow, however, a better indication of the cathode lead of the LEDS would be handy and save time (and a possible mistake). For the reader's information, the cathode lead of the LED is the longer of the two. When mounting the LEDs I recommend placing them about 1/8 of an inch abve the circuit board to prevent damage from overheating during the soldering procedure. Also, while quibbling, the schematic is somewhat misleading as it states the Power LED is different from the others. In my kit there was no indication of a special LED to be used for the Power LED, and the kit seems to perform correctly. The Layout Diagram also has a somewhat confusing statement "Do not cut guides on I/O socket". I'm still trying to figure out what the socket guides are. The assembly instructions, however, caution against cutting the I/O socket pins—and I know what those are. The assembly begins with the mounting of the Tape Guides, a somewhat tricky but not too difficult project. The instructions call for the use of a drill bit to provide the proper clearance and this technique works quite well. The assembly instructions go into great detail concerning the alignment of the sensor. When I assembled my kit there was no difficulty at all.

All told, the assembly took approximately one-half hour from unpacking to finish. I do caution the kit builder to read the instructions, for correct operation does depend upon the alignment of the tape guides and the sensor.

The checkout instructions do not include any information on trouble-shooting, but in my case none was needed. Within five minutes of assembly my kit was completely checked out—however, there is no way given to enable one to checkout the handshaking phase prior to operation of the device with your computer. If you connect the jumper between "A" and "ACK", and connect a 2k ohm resistor between + 5 and the "ACK" line, you can check out this portion of the interface. With the "ACK" line high, advance a piece of tape one sprocket hole; the RDA line should be high. Further advancement of the tape should not cause the RDA signal to change. Now ground the ACK line. RDA should go low until the tape is advanced one more sprocket hole. If your reader passes this test the handshaking circuitry is operational.

Operation of the OP-80A Paper Tape Reader is straight forward. The paper tape to be read is inserted between the guides and pulled from left to right. Note the position of the OAE arrow " ⟩ " and the small sprocket arrow point to the fourth sensor from the bottom for proper tape orientation.

In order to read light weight paper tape (semi-opaque), an LED indicator has been provided to facilitate proper alignment of the light source. (Note . . . A great deal of feedback is utilized in the sensor design to reject the 60 cycle AC component emitted by the light source, however, fluorescent light is *not* recommended as a source.)

To align the reader, place a low wattage incandescent lamp (15 to 60 watts recommended) over the reader and lower until the SP (Sprocket) LED comes on. The OP-80A is now ready for use.

To test the reader, toggle a simple bootstrap loader program into the computer. The program should run in a loop waiting for the RDA line to go high (or RDA to go low.) When the line goes high, the data should be input through the port. If an acknowledge signal is generated by the data input port, it should be sent out over ACK (or ACK). If no acknowledge signal is available, the program must generate one. This may be output through the same port that supplies data to S1 and S2. The program will now return to the initial loop and wait for the next RDA change. (See program given at end of article.)

The parallel interface is very straight forward. The data lines D0 thru D7 are connected to the input port. When data is available, RDA goes HIGH and RDA goes LOW. Either signal may be used to flag the computer through a second input port. After the computer has input the data, it should reset the RDA latch. This may be done with a positive or negative PULSE (ACK or ACK) from a computer output port. This same output port may also control the buffered status LEDS, S1 and S2.

If you do not want to use an output port to reset the RDA latch, you may obtain an ACK (or ACK) signal from the computer input port. This signal is usually the product of a CPU generated "IN" signal, the decoded port address, and a clock timing signal. Refer to your microprocessor manual for details.

Refer to Figure 4 and, using the diagram, connect the reader to a parallel port in the computer.

After connecting the reader to your computer, toggle in the "8080 BINARY LOADER" (or its equivalent if you are using a different processor) and single step through the program to test the interface.

If you encounter difficulty when interfacing the reader, OAE suggests the use of a logic probe to follow the signal paths and operation, however, no trouble-shooting hints are provided.

A serial interface using an UART is provided in Figure 5. OAE provides as software an 8080 Binary Paper Tape Loader and an Intel Format Paper Tape Loader, both of which are included in this article.

When using the OP-80A Paper Tape Reader it is helpful to mount it solidly to prevent it from slipping around when pulling tape. I plan to mount mine to a board to which I also plan to attach tape reels. The reels will be mounted on modified film editors to allow a geared drive to the takeup reel. This will provide a steady motion of the tape through the reader and also provide a place to store the tape. The light-to-sensor distance is somewhat critical and should be fixed securely. OAE indicates that they have a light source available that can be mounted on the Reader itself. No prices or model numbers are given.

The OAE OP-80A Paper Tape Reader provides a low cost method of adding a high speed quiet paper tape input to your computer. It is especially recommended for late night computing when your wife is asleep in the next room.

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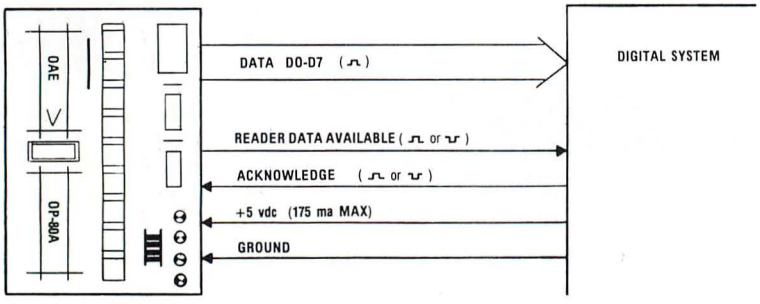
THE OP-80A MAY BE CONNECTED TO ANY MICROPROCESSOR SYSTEM WITH A PARALLEL INTERFACE.



DØ	1	BRN	RED	16	D1
D2	2	ORG	YEL	15	D3
D4	3	GRN	BLU	14	D5
D6	4	VIO	GRY	13	D7
ACK or $\overline{ACK}$	5	WHT	BLK	12	SPARE
$\overline{RDA}$	6	BRN	RED	11	S2
RDA	7	ORG	YEL	10	S1
GROUND	8	GRN	BLU	9	+5vdc

DØ thru D7	DATA OUTPUT BYTE
S1 and S2	STATUS LEDS
RDA	READER DATA AVAILABLE
$\overline{RDA}$	READER DATA AVAILABLE
ACK or $\overline{ACK}$	ACKNOWLEDGE (resets RDA and $\overline{RDA}$)
POWER	+5vdc @ 175ma MAXIMUM

Figure 4.

The Compucolor 8001 System.

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*Unit shown includes light pen and expanded keyboard, both optional at extra cost.

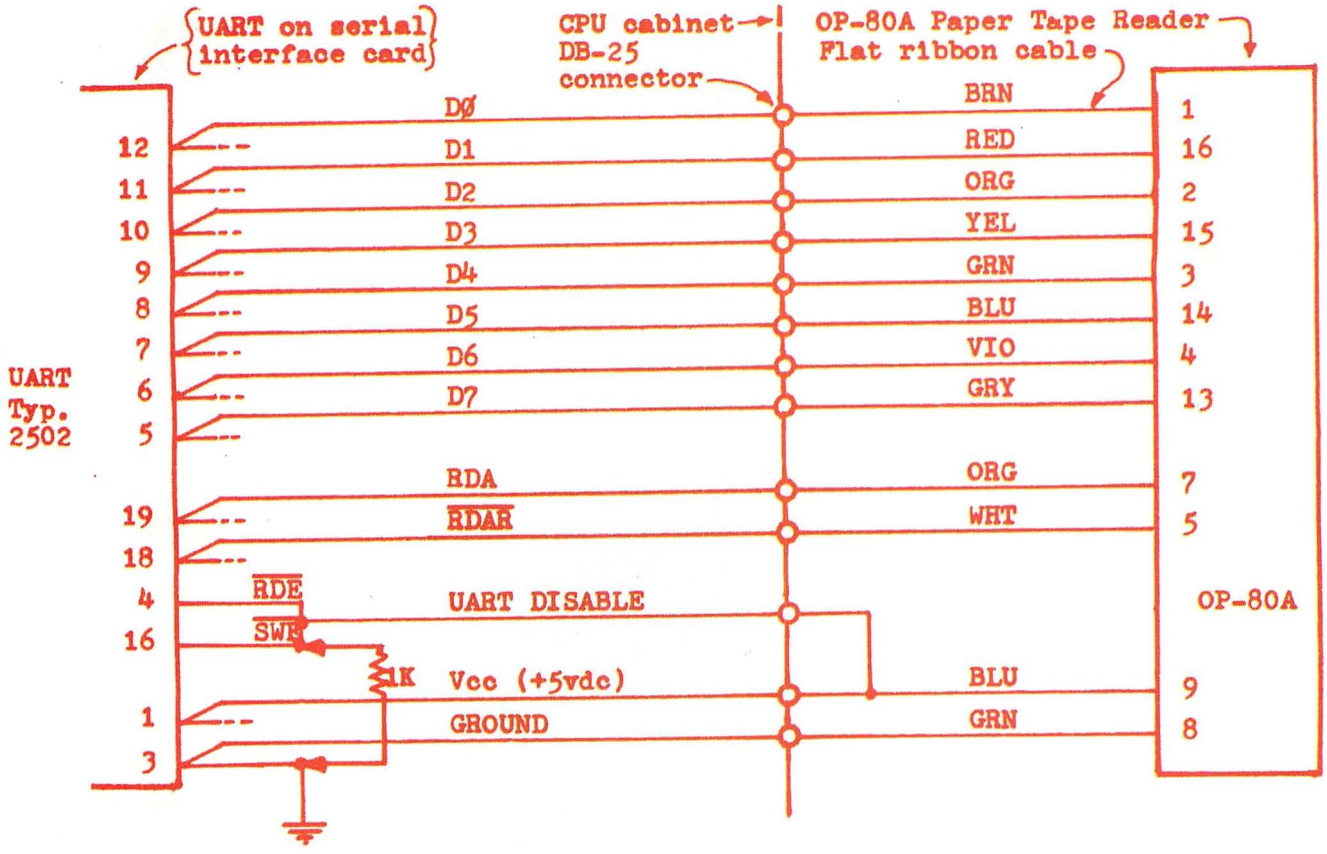
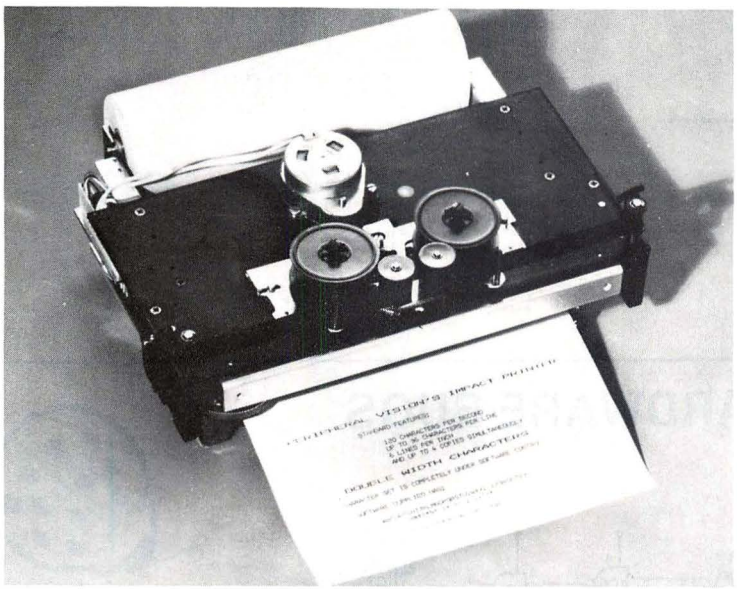


Figure 5.

Peripheral Vision impacts your computer.



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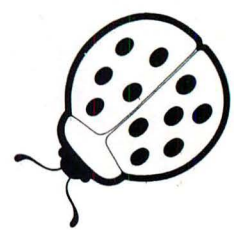
```
FILE
BINRY  3000  35F6

ASSM 0000 2000
0000             0010 *  DATE:   12-01-76          OLIVER AUDIO ENGINEERING
0000             0020 *  TIME:   1400 HRS          NORTH HOLLYWOOD,  CALIF.
0000             0030 *
0000             0040 **********  8080 BINARY PAPER TAPE LOADER  **********
0000             0050 *
0000             0060 *  THIS LOADER PLACES BINARY DATA FROM THE OP-80A
0000             0070 *  IN MEMORY BEGINNING AT THE 'STARTING ADDRESS'.
0000             0080 *  NOTE:   YOU MAY HAVE TO PATCH (MODIFY) THE INPUT
0000             0090 *          PORT NUMBERS AND THE BIT MASK (NOW 80H)
0000             0100 *          TO CORRESPOND TO YOUR HARDWARE CONNECTIONS.
0000             0110 *
0000 21 00 00    0120            LXI   H,0000H     STARTING ADDRESS
0003 DB 00       0130 STBY       IN    0           INPUT READER STATUS BIT (RDA)
0005 E6 80       0140            ANI   80H         DROP (MASK) ALL BUT RDA STATUS BIT
0007 CA 03 00    0150            JZ    STBY        WAIT FOR FIRST DATA BYTE
000A DB 01       0160            IN    1           INPUT DATA BYTE
000C B7          0170            ORA   A           SET ACCUM STATUS FLAGS
000D CA 03 00    0180            JZ    STBY        WAIT FOR FIRST NON-ZERO DATA BYTE
0010 77          0190 STUFF      MOV   M,A         STORE DATA AT LOCATION HL
0011 23          0200            INX   H           INCREMENT MEMORY POINTER
0012 DB 00       0210 WAIT       IN    0           INPUT READER STATUS BIT (RDA)
0014 E6 80       0220            ANI   80H         DROP ALL BUT STATUS BIT
0016 CA 12 00    0230            JZ    WAIT        WAIT FOR DATA
0019             0240 ************************************************
0019             0250 *  THE FOLLOWING ROUTINE IS NOT REQUIRED IF THE
0019             0260 *  INTERFACE GENERATES AN ACKNOWLEDGE SIGNAL.
0019 3E 80       0270            MVI   A,80H       SET ACKNOWLEDGE BIT HIGH
001B D3 02       0280            OUT   2           OUTPUT ACK SIGNAL
001D 2F          0290            CMA
001E D3 02       0300            OUT   2           REMOVE ACK SIGNAL
0020             0310 ************************************************
0020 DB 01       0320            IN    1           INPUT READER DATA
0022 C3 10 00    0330            JMP   STUFF
2000             0000 * DATE:  12-01-76
2000             0010 * TIME:  1200 HRS
2000             0020 *
2000             0030 * THIS IS THE INTEL FORMAT PAPER TAPE LOADER.
2000             0040 *  YOU MAY NEED TO PATCH THE STACK POINTER
2000             0050 *  AND TTYIN LOCATIONS FOR YOUR SYSTEM.
2000             0060 *
2000             0070 *  INITIALIZE THE STACK POINTER
2000 31 00 4D    0080            LXI   SP 4D00H
2003 CD 06 20    0090            CALL  READ
2006             0100 *  INPUT BLOCK LENGTH AND ADDRESS
2006 CD 45 20    0110 READ       CALL  TTYIN
2009 FE 3A       0120            CPI
200B C2 06 20    0130            JNZ   READ
200E CD 2A 20    0140            CALL  CHAR
2011 57          0150            MOV   D,A
2012 C8          0160            RZ
2013 CD 2A 20    0170            CALL  CHAR
2016 67          0180            MOV   H,A
2017 CD 2A 20    0190            CALL  CHAR
201A 6F          0200            MOV   L,A
201B CD 2A 20    0210            CALL  CHAR
201E             0220 *  INPUT BLOCK OF DATA
201E CD 2A 20    0230 LOOP       CALL  CHAR
2021 77          0240            MOV   M,A
2022 23          0250            INX   H
2023 15          0260            DCR   D
2024 C2 1E 20    0270            JNZ   LOOP
2027 C3 06 20    0280            JMP   READ
202A             0290 *  CONVERT ASCII TO BINARY
202A CD 45 20    0300 CHAR       CALL  TTYIN
202D CD 3D 20    0310            CALL  HEX
2030 07          0320            RLC
2031 17          0330            RAL
2032 17          0340            RAL
2033 17          0350            RAL
2034 5F          0360            MOV   E,A
2035 CD 45 20    0370            CALL  TTYIN
2038 CD 3D 20    0380            CALL  HEX
203B 83          0390            ADD   E
203C C9          0400            RET
203D             0410 *  CONVERT HEX (A-F) TO BINARY
203D D6 30       0420 HEX        SUI   30H
203F FE 0A       0430            CPI   0AH
2041 D8          0440            RC
2042 D6 07       0450            SUI   07H
2044 C9          0460            RET
2045             0470 *  INPUT HEX FORMATTED DATA FROM OP-80A
2045             0480 *  AND ECHO TO TERMINAL.  (DELETE THE OUT COMMAND
2045             0490 *  IF YOU WISH TO LOAD TAPE AT HIGH SPEED!)
2045 DB 00       0500 TTYIN      IN    0
2047 E6 80       0510            ANI   80H
2049 CA 45 20    0520            JZ    TTYIN
204C DB 01       0530            IN    1
204E D3 01       0540            OUT   1
2050 E6 7F       0550            ANI   7FH
2052 C9          0560            RET
```

HARDWARE BUGS



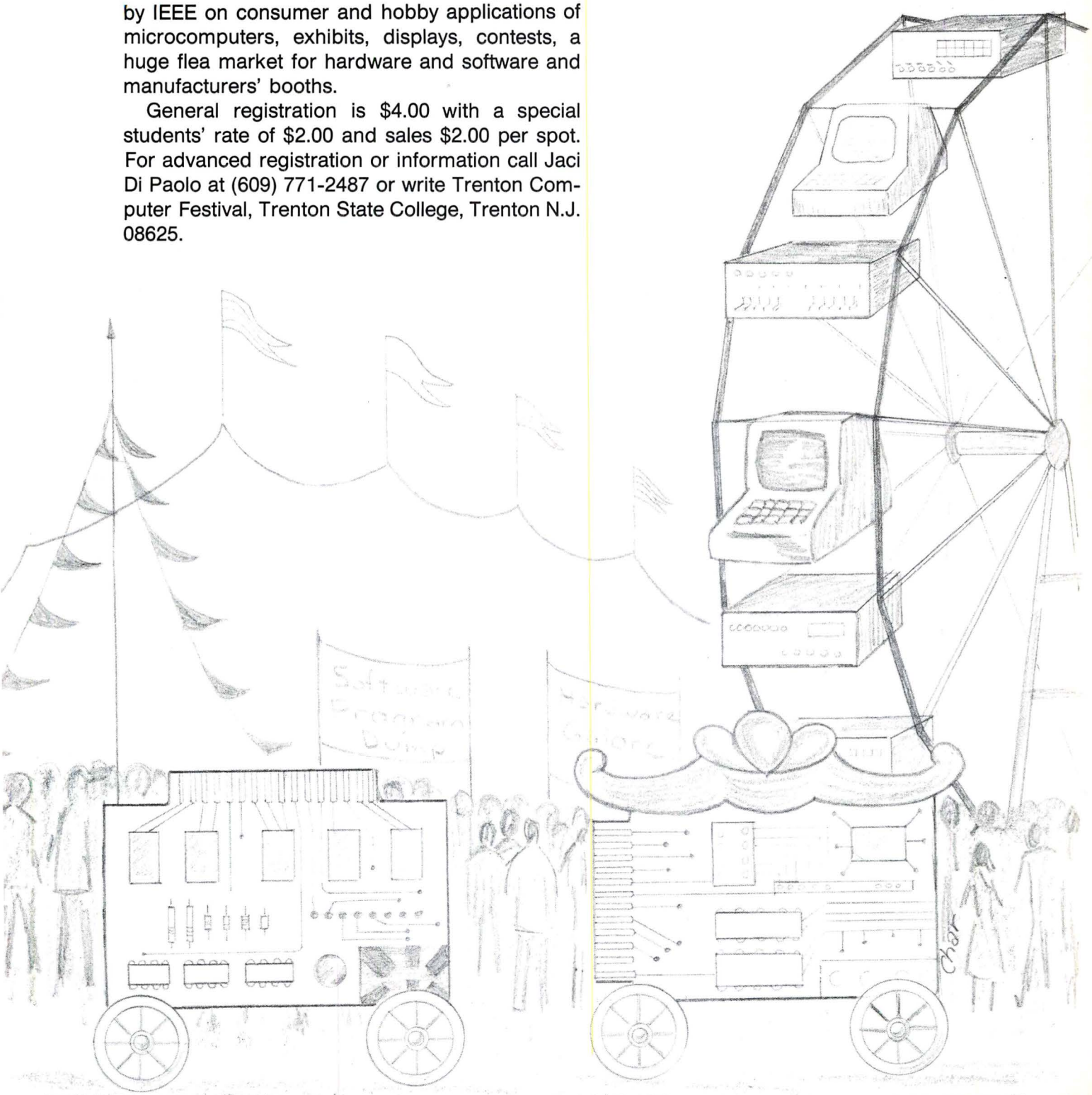
Readers who enjoyed Roger W. Brown's article in the February issue on *Building a 12-Bit A/D Converter* should refer to the revised schematic. Some errors occurred in the original on page 47.

TRENTON COMPUTER FESTIVAL

The Second Trenton Computer Festival will be held at Trenton State College, Route 1, Tenton, N.J. from April 30, 1977 to May 1, 1977.

Featured are a special conference sponsored by IEEE on consumer and hobby applications of microcomputers, exhibits, displays, contests, a huge flea market for hardware and software and manufacturers' booths.

General registration is $4.00 with a special students' rate of $2.00 and sales $2.00 per spot. For advanced registration or information call Jaci Di Paolo at (609) 771-2487 or write Trenton Computer Festival, Trenton State College, Trenton N.J. 08625.



Programmable Bit-Rate Generator

By Krishna Rallapalli

The industry standard Universal Asynchronous Receiver/Transmitter (UART), an MOS/LSI subsystem, has had a considerable impact on data-communication system design. Not only has the UART dramatically reduced chip counts and increased reliability, etc., but it has also provided an incentive to integrate the remaining support functions.

One such subsystem is the 34702 programmable bit-rate generator, designed to provide the necessary clocking signals to operate asynchronous transmitter and receiver circuits. Several standardized signaling rates are used for start-stop communication depending on the transmission medium and other system requirements. The equipment must be capable of generating all the necessary frequencies and provide a way to select the desired one. In the past, this required several SSI/MSI circuits. Now, the 34702 can perform the task more easily and economically.

The 34702 provides any one of the 13 common bit rates on a selectable basis using an on-board oscillator and an external crystal; it also is expandable for multichannel applications. In its most general form, multichannel clocking requires that any of the possible frequencies must be available on any channel. Expansion up to eight channels is accomplished without device duplication. In multiple-device systems, there is no need to use a crystal with every device. *Figure 1* shows the block diagram of the 34702 which consists of the following major parts:

- Oscillator and associated gating
- Scan counter
- Count chains
- Initialization circuit
- Multiplexer and output storage

OSCILLATOR AND ASSOCIATED GATING

The oscillator circuit together with an external crystal generates the master timing. A 2.4576 MHz crystal provides 16 times the frequency of the baud values marked; for example, 9600 baud corresponds to 153.6 kHz. If the External Clock Enable (E_{CP}) is HIGH, the oscillator output signal drives the

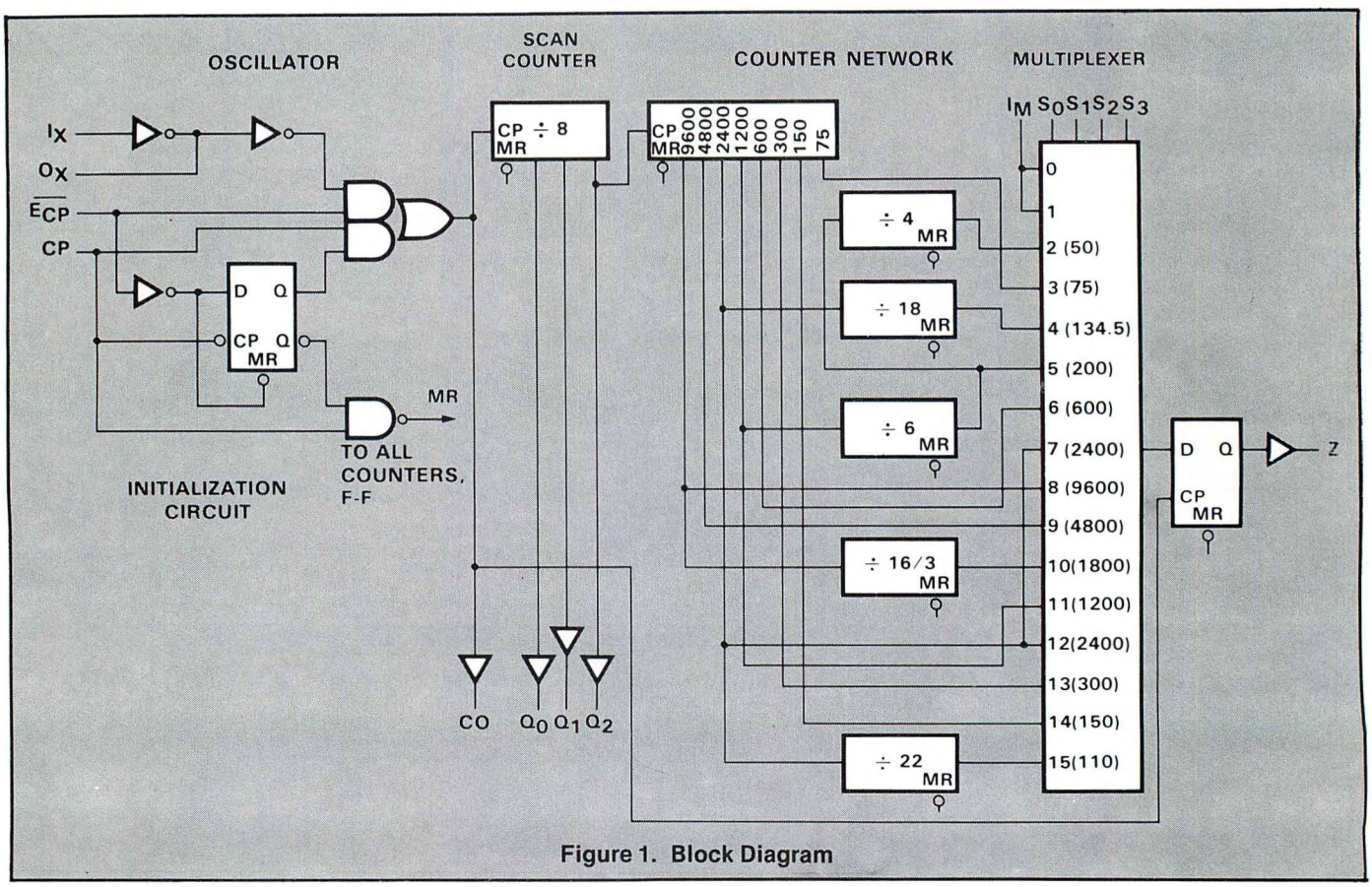


Figure 1. Block Diagram

count chain. On the other hand, if it is LOW, the External Clock (CP) signal is enabled and is then the timing source. The External Clock input also participates in the device initialization scheme. The master timing signal, either from the external source or the local oscillator, is available on the Clock Output pin (CO). This signal can be used to drive other 34702s in a multiple device system, thus eliminating the need to provide more than one crystal.

SCAN COUNTER

The master timing drives a 3-bit binary Scan Counter which, in turn, drives the remaining counter chains on the chip. The Scan Counter allows expansion to eight channels as described later. The prescaling feature of this counter provides another benefit, *i.e.*, it moves the input frequency to 2.4576 MHz which is ideal for low-cost crystals. If it were not for the scan counter, the 34702 would require a more expensive crystal of about 300 kHz.

COUNT CHAINS

The Scan Counter output drives an 8-bit binary counter which provides the frequencies corresponding to 9600, 4800, 2400, 1200, 600, 300, 150 and 75 baud. The 1800-baud signal is generated by dividing 9600 by 16/3. The 110 and 134.5 baud signals are approximated by dividing 2400 by 22 and 18 respectively. Dividing 1200 by 6 gives the 200 baud signal, while 50 baud is generated by dividing 200 baud by 4. All division factors except 16/3 are even; thus, all outputs except 1800 baud have a 50% duty cycle.

The actual division by 16/3 is achieved by using a sequence of integers 5 and 6 such that cumulative error after every three cycles is zero. This scheme, in conjunction with the divide by 16 performed in the UART, achieves good timing accuracy demanded by high speed communication equipment. Calculations indicate that the maximum distortion introduced does not exceed 0.78% regardless of the number of elements in a character.

INITIALIZATION CIRCUIT

This circuit generates a Master Reset signal to initialize the flip-flops on the 34702 to a known state. If the External Clock Enable ($\overline{E}_{CP}$) is LOW, the local oscillator output is inhibited and timing is derived from the External Clock (CP). The first positive half cycle of the External Clock is used to generate the Master Reset and all succeeding clock signals are used for timing. This initialization scheme allows software-controlled diagnosis for fault isolation.

The External Clock can be a software generated signal, *e.g.*, setting and resetting a flip-flop. This provides an effective "single-clock" operation mode. Since the reset forces all counters of the 34702 into a known state, simple software can analyze the system behavior after a given number of clock pulses. In general, if the clock were free running, software has meaningful control only at the character boundaries.

Table 1
Truth Table For Rate Select Inputs

S_3	S_2	S_1	S_0	OUTPUT RATE (Z)
L	L	L	L	MULTIPLEXED INPUT (I_M)
L	L	L	H	MULTIPLEXED INPUT (I_M)
L	L	H	L	50 BAUD
L	L	H	H	75 BAUD
L	H	L	L	134 5 BAUD
L	H	L	H	200 BAUD
L	H	H	L	600 BAUD
L	H	H	H	2400 BAUD
H	L	L	L	9600 BAUD
H	L	L	H	4800 BAUD
H	L	H	L	1800 BAUD
H	L	H	H	1200 BAUD
H	H	L	L	2400 BAUD
H	H	L	H	300 BAUD
H	H	H	L	150 BAUD
H	H	H	H	110 BAUD

MULTIPLEXER AND OUTPUT STORAGE

All the desired outputs from the count chains are fed as data inputs to a multiplexer. The select inputs for this multiplexer are brought out as Rate Select inputs (S_0 - S_3). *Table 1* shows the correspondence between this code and the resulting frequency. The multiplexer output is fed as data input to a resynchronizing flip-flop that is clocked by the leading edge of the master timing.

If only single-channel applications of the 34702 were considered, the output flip-flop would be unnecessary. In multichannel applications, however, the Rate Select inputs change as a function of the Scan Counter outputs (Q_0 - Q_2). The resynchronizing flip-flop assures a fixed timing relationship between Q_0 - Q_2 and the Bit Rate output (Z).

Three important features should be noted from *Table 1*. First, two of the select codes specify Multiplexed Input (I_M) signal as the data source to the multiplexer. The user can feed a signal into this input, however, the primary intent was to feed a static logic level to achieve a "zero baud" situation. Secondly, the codes corresponding to 110, 150, 300, 1200 and 2400 baud each have a maximum of only one LOW level. These are the most commonly used rates in contemporary data terminals. Thus the rate select mechanism on these terminals need only be a single-pole 5-position switch with the common terminal grounded. Thirdly, 2400 baud is selected by two different codes so that the whole spectrum of modern communication rates will have a HIGH code in the most significant bit position.

TYPICAL APPLICATIONS

In those applications where the Rate Select inputs are static levels, operation of the 34702 is rather straightforward. The multiplexer connects the specified counter output to the data input of the output flip-flop. Because the flip-flop is clocked by the master timing, its output reflects the selected frequency.

SINGLE-CHANNEL BIT-RATE GENERATOR

Figure 2 shows the simplest of all 34702 applications. This circuit provides one of five possible bit rates as determined by the setting of the 5-position switch. The generated frequencies correspond to 110, 150, 300, 1200 and 2400 baud depending on the switch setting. For many low cost terminal applications, these five selectable bit rates are adequate. The 34702 is not only intended for single-channel but also for multichannel operation, as illustrated in the following applications.

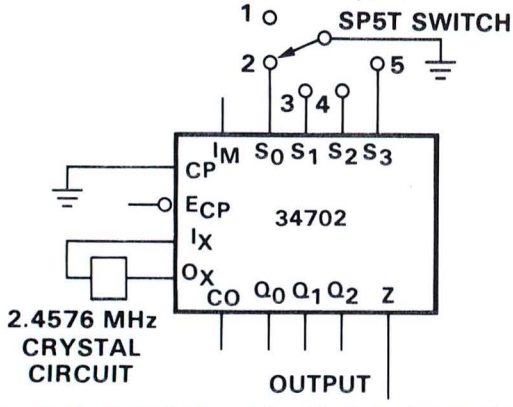


Figure 2. Switch Selectable Bit-Rate Generator Configuration Providing 5 Bit Rates

MULTICHANNEL BIT-RATE GENERATION

Figure 3 illustrates a fully programmable channel bit-rate generator system. Two 4 x 4 register file devices (9LS170) can be loaded with information (rate select codes from *Table 1*) relating to the desired frequency on a per-channel basis. For clarity, circuits for writing into the files are not shown.

The least significant Scan Counter outputs (Q_0, Q_1) control the Read Address of the 9LS170s while the most significant output (Q_2) controls the Read Enable (RE) inputs. Thus, as the counter advances, file locations are read out sequentially. The Scan Counter outputs are also the Address inputs for the 93L34 addressable latch. The Bit Rate output (Z) of the 34702 is the Data input to the 93L34 while the Clock Output is the Enable input.

To understand the operation, consider the instant when the Scan Counter outputs become Zero (Q_0 - Q_2 = LOW). The same clock that incremented this counter to Zero also

clocked the counter output, corresponding to the selected frequency for channel 7 into the output flip-flop, and

disabled the 93L34 latch via the Clock Output

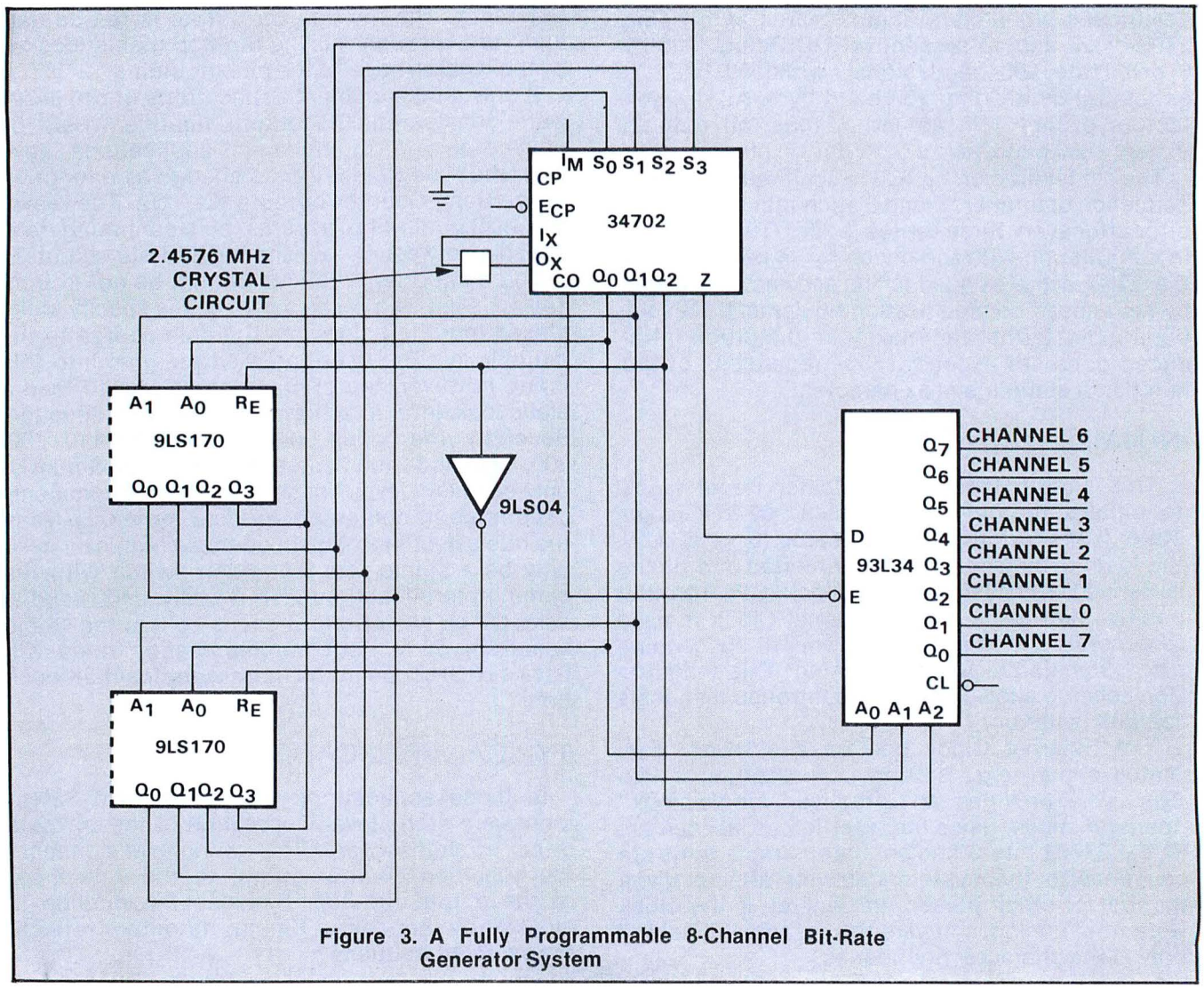


Figure 3. A Fully Programmable 8-Channel Bit-Rate Generator System

(CO), thus preventing any change in the latch outputs while the Scan Counter outputs and the Bit Rate output (Z) are changing.

During the second half of the clock cycle, when the Clock Output (CO) is LOW, the counter output representing the selected frequency for channel 7 is loaded into the 93L34 latch and is locked up on the Q_0 output.

The Scan Counter outputs (Q_0 - Q_2), which represent the selected channel, are used to interrogate the register file to determine the assigned bit rate for channel O. The stored code for channel 0 is routed to the Rate Select inputs (S_0 - S_3) to select the appropriate internal frequency, so that during the next LOW-to-HIGH clock transition, the state of this internal signal is clocked into the output flip-flop. Thus, each channel is sequentially interrogated and the 93L34 latch is updated at least once during each half cycle of the highest output frequency (9600 baud).

By connecting the Scan Counter output Q_2 to the Multiplexed input (I_M) a similar technique can be used to implement a system with a maximum output frequency of 19,200 baud, however, the number of channels must be limited to four. This ensures that the output will be interrogated and updated at least once during each half cycle of the highest output frequency (19,200 baud).

JUMPER PROGRAMMABLE 8-CHANNEL BIT-RATE GENERATOR

In systems where channel-speed assignments remain relatively fixed, software-controlled channel assignment is not necessary or practical. It may be simpler to program with "jumpers" at appropriate places in the system. See *Figure 4.*

In the jumper programmable 8-channel bit-rate generator, the scan counter outputs (Q_0 - Q_2) are fed as Address inputs to a 93L01 decoder and a 93L34 addressable latch. The decoder outputs drive the diode clusters which contain four diodes for each channel. All four diode cathodes in a cluster are connected together to a decoder output; the anodes of corresponding diodes in every cluster are connected together to the appropriate Rate Select inputs of the 34702. Presence of a diode results in a LOW on the particular 34702 input; when a diode is absent, a HIGH results. As the scan counter advances, the decoder outputs activate the desired bit-rate code for that channel. The 93L34 synchronously demultiplexes the 34702 output (Z) and reconstructs the specified bit rates at its output.

CLOCK EXPANSION

The basic 34702 can be expanded to a maximum of eight channels. In applications where more than eight channels are needed, the 34702 must be duplicated. The device is designed with a clock-expansion feature; therefore only one crystal is required to operate all the channels.

The most economical expansion scheme provides one 34702 with a crystal and all other devices derive their timing from this master. The device wiring is such that the External Clock Enable input and I_x input of all but the master device feeds

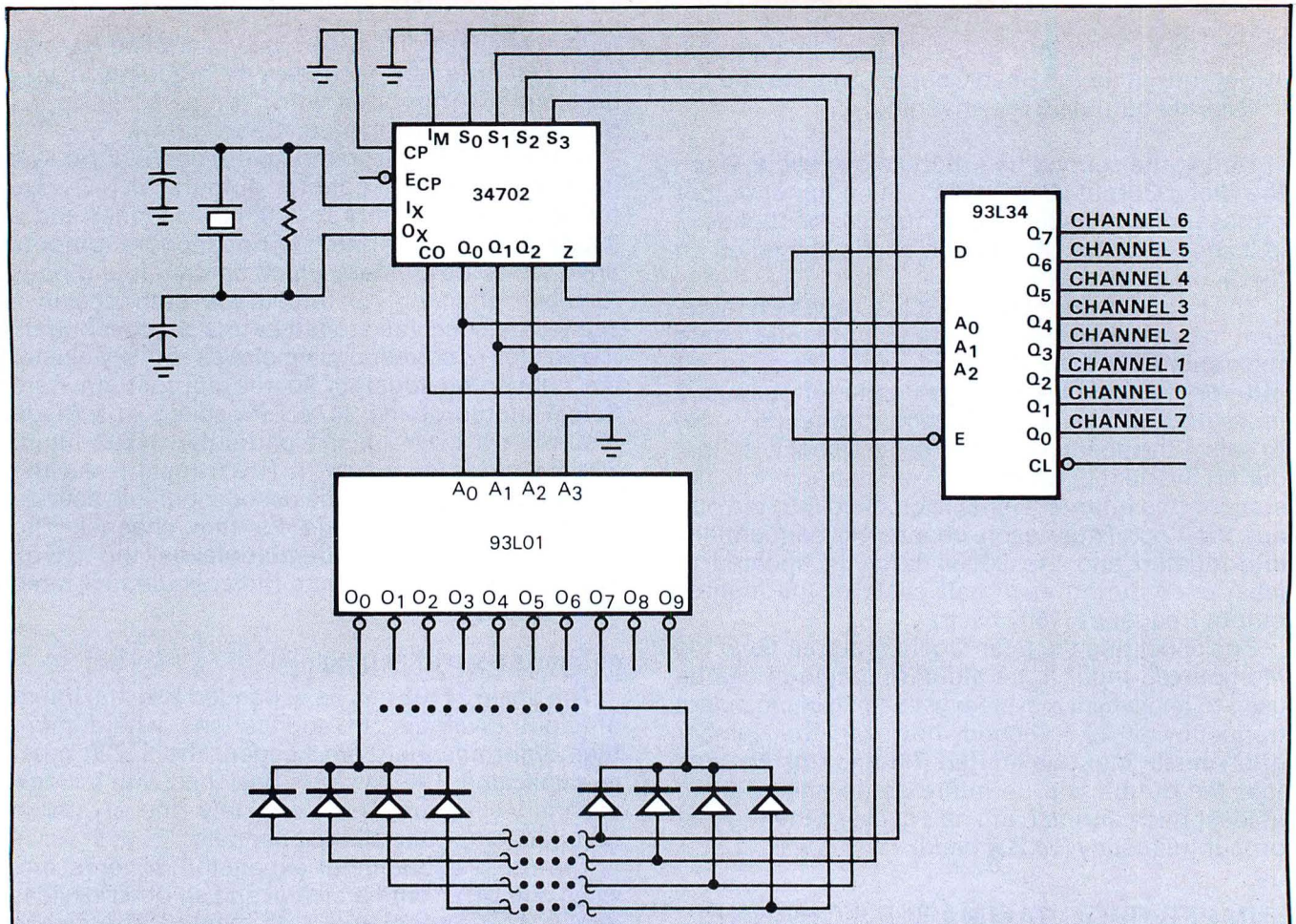


Figure 4. Jumper Programmable 8-Channel Bit-Rate Generator

into the External Clock input of all the other devices. The Clock output of each device is connected to its associated 93L34 Enable input as before. An alternative scheme is shown in *Figure 5.*

The advantage of this scheme is that it can be conveniently used to implement the software external clock feature mentioned previously. Imagine that the External Clock Enable (E_{CP}) inputs of all the 34702s in the system are controlled by the output of a flip-flop (mode) and the External Clock inputs (CP) of all the devices are tied together and software driven, possible by operating another flip-flop. During normal operation, the mode control is HIGH, thus selecting the crystal oscillator for timing. Also, the external Clock input of each device is held LOW. When the External Clock Enable goes LOW, in preparation for the diagnostic mode, all devices receive their timing from the External Clock input. When this input goes HIGH for the first time, all devices generate an internal Master Reset signal clearing their counter chains. The next HIGH-to-LOW transition sets the internal control flip-flop and thus terminates the Reset; all counters are free to start counting in response to the External Clock signal.

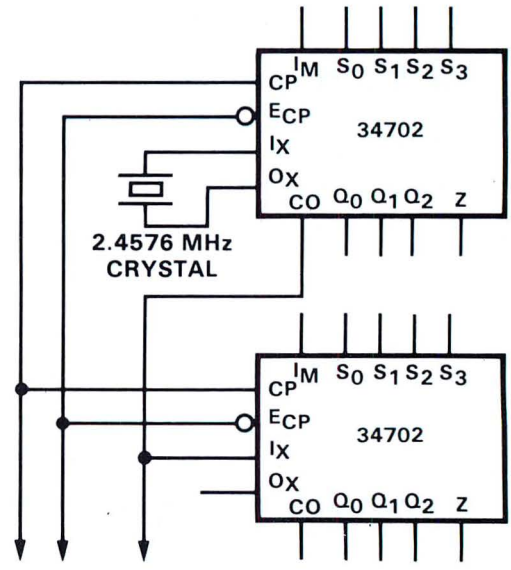


Figure 5. Tandem Clock Expansion Scheme

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Building a Digital Group System

by Donald O. Southwick

I've had a long-standing interest in electronics that goes back to the venerable days of the #80 rectifier tubes, but had never worked in the field, much less thought of playing in it. A few years ago my interest was low key until my son got beyond the switches-and-light-bulb stage, then I found out that ICs were real and not expensive. Together we built a kit calculator, 555 timers, numerous decade counters, a digital clock and many other gadgets.

About this time microcomputers made the press in various magazines, and the devices aroused my interest. However, gathering information in those days was another matter. Hobby computerism was almost an underground movement. At last about two years ago the Digital Group was formed in Denver and I found other people of like interest. Most club members, however, knew much more than I, and it soon became clear to me that if I was to learn abut computers, I would have to build one. Besides, my son was playing with a terminal at school and I was yet to throw a switch on one.

Father and son with a little hardware background and absolutely no software background charged into the project.

Decision, frustrations and delays. . .

Now we have an operating system and I couldn't be more pleased. There's much more to learn; a whole new world lays ahead to conquer. I couldn't be more pleased. . .

The Digital Group had kept a low profile and took a long time to get their systems ready. For the hobbyist who is shy about small companies who operate out of post office boxes, I can say that I found them competent and honest. Of course the other side of the low-overhead, low-profit-margin picture is their inability to handle large numbers of inquiries with efficiency. Hence my system took three months longer than planned to be completed.

My system is a T.V./keyboard/cassette based with 8080A, 6800, 6502 and now a Z-80 CPU core. A minimum system consists of three or four 12" x 5½" plugable boards and a mother board, possessing either four or nine slots. Equipment included power supplies, a commercial T.V. monitor, cassette recorder, a computer-controlled tape deck and an impressive line of cabinets (See Photo 1).

I can highly recommend all the components. They have all proved reliable and easy to work with. The hobbyist especially appreciates the fact that this equipment is designed to be expandable and interchangeable. To change CPUs simply unplug the CPU board in the unit and plug in the CPU board you want, read in the appropriate operating software from cassette and you are operating again in a matter of minutes.

THE CPUs

On the bare board level the 6800 and 6502 share the same board. All CPUs contain the first 2K of RAM (2102 or equivalent) and a programmed EROM (1702A). The EROM enables you to operate your cassette software and to display your output on the T.V. monitor without an additional memory board.

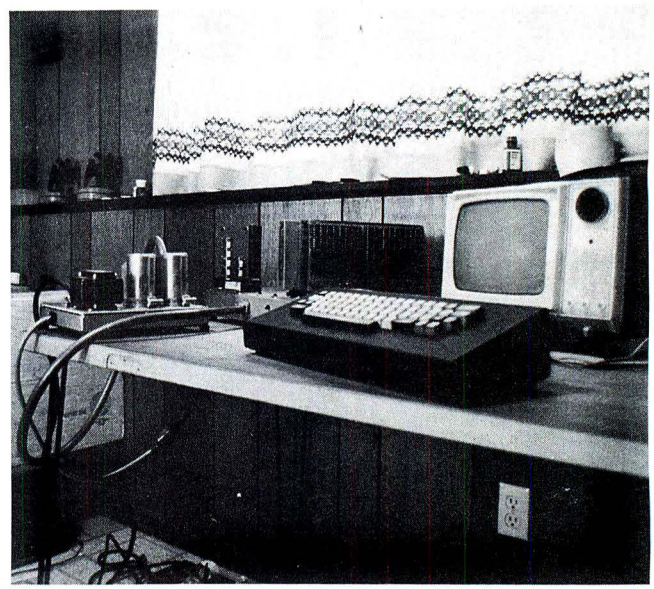


Photo 1. System Complete.

T.V. CASSETTE BOARD

The T.V. board generates a picture 16 lines high by 32 characters wide for 512 spaces. The Motorola 6571L provides upper and lower cases and Greek-math symbols (see Photo 2). This board can be used as a stand-alone with the keyboard and T.V. The cassette interface on the right side of the board is designed for frequency shift keying and uses a relatively high ratio of discrete components. This section must be tuned with a calibrated A.F. generator and, although the procedure is well described and not tricky, the necessary equipment may not be available to the hobbyist. Digital Group will tune your board for a fixed fee.

IN/OUT BOARD

I recommend to start the project by building this board; it is the easiest one in the system. Each I/O provides four output ports, each an 8-bit parallel. On the first I/O, 1-1/8 ports (in and out) are used by the TVC keyboard and cassette. The rest is uncommitted.

MEMORY BOARD

Any expansion of a system is likely to include an 8K static RAM board. Digital Group's product has 64 2102s (or equivalent) and five other ICs. It is a very tightly packed board with over 1,100 solder connection. Don't let that scare you off, however. My 13-year-old son, with little soldering experience, did mine with no problem. Jumpers are used for different addresses — first 8K, second 8K onward. Pads are even provided for pull-up resistors.

Photo 2. TV Display Showing TV Format and What the Character Generator Will Do.

MOTHER BOARD

My *standard* (Photo 3) mother board measures 10-3/8" by 12" and has space for four I/Os or peripherals, for three 8K memories, for the TVCs and the CPUs.

The smaller four-slot mother board measuring 5-3/8" x 12" is the center section of the larger board and has space for only one I/O, one memory and TVC and CPU. Pads for jumpers are provided on both mother boards to jump to available memory or to I/O expansion. Besides the data and address busses and power connections, the mother board connect the TVC and CPU and the I/O. No point-to-point wiring is required within the system. Each socket on the mother is wire-wrap type and a special Molex socket is used to connect to the ends of the wire-wrap.

T.V.

Economics dictated my choice there. The hobbyist usually has to satisfy himself with dismantling the discarded old tube type. With so little experience I was reluctant to modify even that for direct video output. With some background education and a Sams schematic, I took courage. Once started I found the task surprizingly easy (Photo 2 and 4).

KEYBOARD

The keyboard I used was a ACSII encoded surplus unit with upper and lower case capability. The cabinet is home-made. I had trouble with the keyboard probably because of the length and type of cable I used. On first runs it was voltage sensitive; at optimum voltage there were too many "no entries" or multiple entries. After running the strobe pulse through both halves of a 7413 Schmitt trigger located near the input port, it is much improved.

CHASSIS

The power chassis is a 1" x ½", 18" aluminum channel frame with an aluminum plate on top and a clear plastic plate on the bottom. There is no voltage exposed, but I can still look for a smoke source (Photo 5). The main chassis at 13¼" x 17" is planned for expansion and is made from 2" x 1" aluminum channel with one end reversed

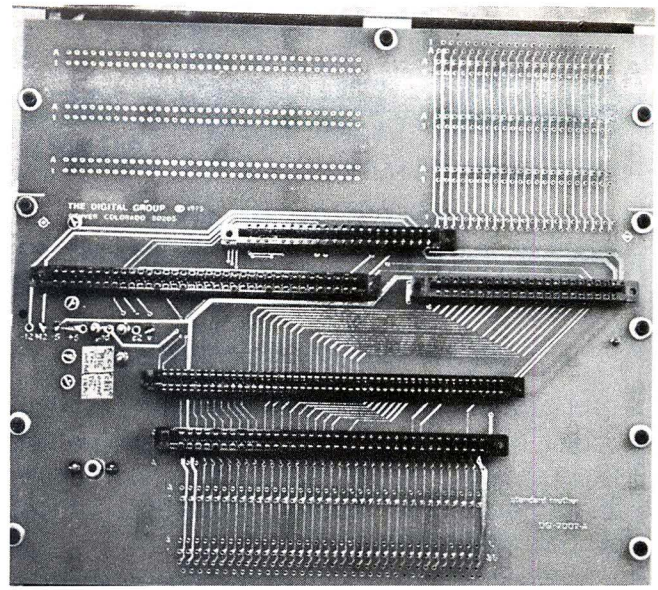


Photo 3. Mother Board Top View. Top to Bottom—3 Spaces for Peripheral or L/O Boards, TVC, I/O, CPU, Memory, Spaces for 2 More Memory Boards. Smaller Mother Board is Like This but Cut Off Just Above and Below Existing Sockets.

Photo 4. Option List Displayed on TV From Supplied Operating Software.

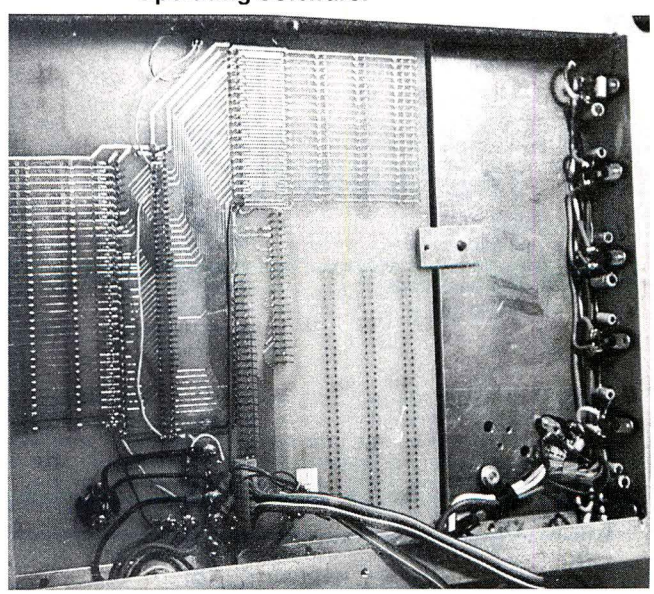


Photo 5. Bottom View of Main Chassis Mother Board In Center, a Molex Socket on End of a Ribbon Cable Connecting Keyboard. On End, Back of Regulators.

and drilled for six TO-3 regulators. An aluminum panel 5¼" wide over the regulator end adds rigidity, mounts the fuse panel and provides room to mount smaller than board-size devices. A gap is left at both ends of the mother board for wires or ribbon cable to be brought up.

POWER SUPPLY

Built on a separate chassis the power supply was designed around three available surplus units. The foot-operated power switch is on the supply chassis and no AC is on the main chassis. A switched and fused three-wire line goes to the T.V. This + 12V system will provide sufficient power for further expansion.

In-line bridge rectifiers are used and are mounted in pairs by sandwiching them between the plate and the chassis using silicone grease for maximum heat-sinking (Figure 1). The power plug might be of interest to hobbyists: it is a Hubbell (#5280) three-wire plug with a thumb screw on the ground pin locking it into any standard three-wire outlet to prevent accidental unplugging. Listing at over $4.00, it is somewhat expensive, but a good idea to prevent accidental loss of a program on which you have invested hours of work.

Editor's note: The power supply described here is Mr. Southwick's design and not supplied by Digital Group.

P C CARD

Voltage regulators (LM-309s, 320s and 340s) are mounted on end of the main chassis (Photo 6). I decided to use a separate + 5V regulator for each board and fuse the line from each regulator. I also installed 5W Zener diodes on each board at each voltage, (5.6 IN 5339 for ± 5V and IN 5352 for ± 12V) for overvoltage and reverse polarity protection. Excessive voltage drop occurred across the fuses which caused me to increase the fuse rating to about three times the nominal current. This however somewhat decreased the protective value of the original arrangement.

In time I have had to rework some of the regulator section. Present memory is now 10 K and growing. Increased current demands cause excessive heat build-up on that end of the chassis. This has been partly solved by moving some of the regulators to a heat sink mounted on the fuse mounting brackets above the chassis plate. The next step will have to be LM 323s (5V @ 3A) regulators or pass transistors, which may also let me consolidate some of the clutter.

DOCUMENTATION

A good-sized stack of unbound paper comes with the system. Some of what I received had omissions and mistakes, but by now they have been corrected. It is not comprehensive on computer architecture, nor software, nor does it teach you how to solder, but it does instruct you sufficiently to build if you have some hardware experience and access to test equipment.

Each board comes with its own leaflet which contains a circuit description, assembly instructions, trouble-shooting notes, parts lists, diagrams and schematics. A systems and operating manual provides overlap information on the mother board, overall construction cues, information on the bus structure, pin assignment, an 8080 instruction set and material on cabinets, cassettes, and T.V. monitors. The operating software and demonstration programs on the cassette provided with the system are also described.

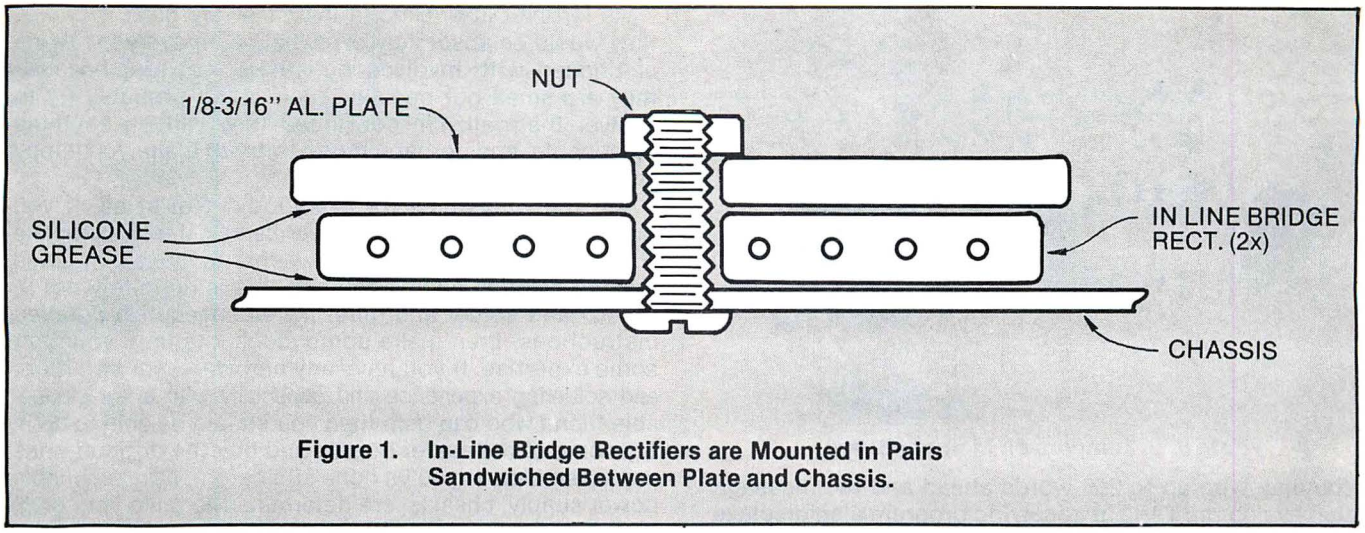


Figure 1. In-Line Bridge Rectifiers are Mounted in Pairs Sandwiched Between Plate and Chassis.

OPERATION/SOFTWARE

This is where it's hard to stay calm. The TV/keyboard approach, combined with the software you get on cassette takes the work out of having fun. Power up, push "reset", read in cassette, watch the pages load, and, in less than a minute, you may select from the four options displayed (Photo 4) by simply pressing the corresponding number on the keyboard.

1. Read Cassette
2. Write Cassette
3. T.V. Storage Dump
4. Keyboard Program
5. Your Title

1. Read Cassette: Allows you to read in additional programs while you watch the words load on the TV.

2. Write Cassette: Outputs to a recorder while the T.V. displays "Cassette being written". Besides the obvious value of being able to store and duplicate programs, before you run an untried program, put it on tape. If it self-destructs, you still have it, can read it back, look it over, and make necessary changes. After using this, or the other options, you can return to the display for another choice.

3. T.V. Storage Dump: This will first show the register, flag, stack, and status, then, by pressing the space bar, you may page through memory, 96 bytes at a time, in octal. By pressing "S" the T.V. will display "Page address" and by keying in 007, for example, it will start displaying memory at page 7 and you may proceed paging through from that point. Press "R" and you return to the option display, press "P" and go to the programing routine.

4. Keyboard Program: This lets you program in octal from the keyboard. Normally this starts on page 6, but it can be modified, or you may select an address. Of course, what you program is displayed as you do it, with address, and with several preceding addresses and their contents. "S" will put you back to the "Storage Dump" mode and "R" to the option display.

5. ————————: You can fill in your own title. It does whatever program you put in starting at page 6, 6/8ths of the way through the first 2K of memory. The operating software being described is in the first 1½K. There is room in this format for from five to ten option programs if you don't exceed the available memory.

Included in this software are several subroutines you can call and use in your own programs. These include T.V. display, T.V. erase, keyboard, a timing loop and others.

If this is insufficient, there are four more programs on the cassette. There is a Morse code sending and receiving program, requiring some external hardware, which will send code at a rate you select while you type the message.

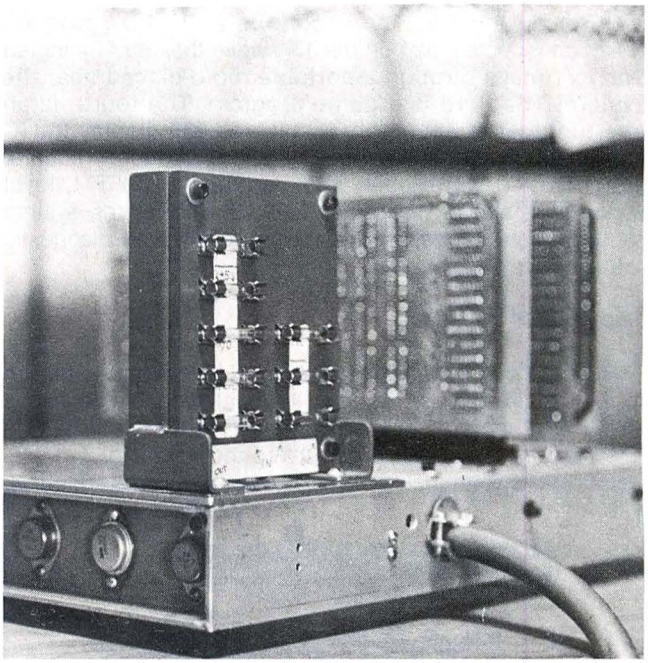


Photo 6. Main Chassis Showing Regulators and Fuse Block.

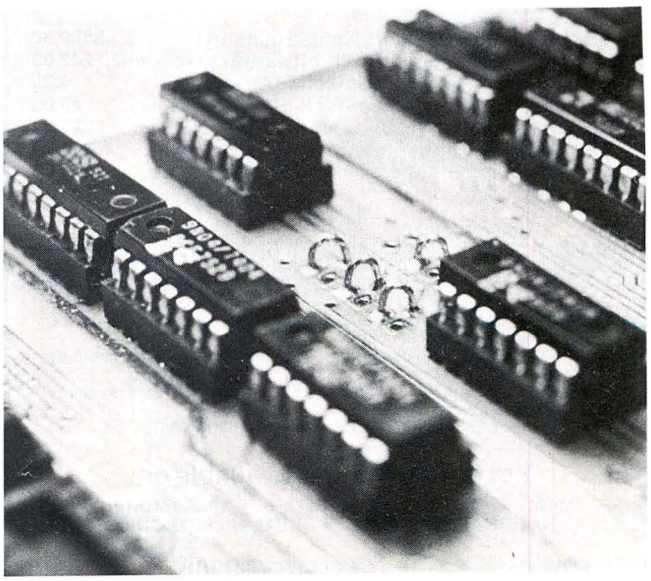


Photo 7. Jumpers on I/O Board, Zener in Background Is Homebrew.

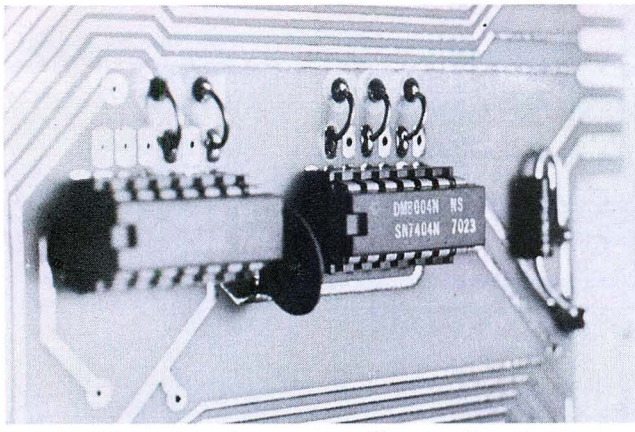


Photo 8. Jumpers on Memory Board.

You may type up to 256 words ahead and the message displays on the T.V. The receiving program also displays the received message, for example, from a shortwave receiver on the T.V. The second is a "FLAG" program which constructs a flag on the T.V. while the "Star Spangled Banner" plays through a portable radio placed near the system! The third is a game program. The fourth is an interrupt test — a memory test which will display the IC number of any defective memory, and a frequency counter circuit which will display the frequency of a TTL level conditioned signal. Besides interrupt capability the system can be single-stepped and some more involved diagnostic routines are described.

CONCLUSION

Do I like the system? Yes, I do and I have barely begun to use its potential. In fairness, I would probably be happy with the other available systems too, but I feel this one has the most favorable pleasure-to-money ratio.

As for the Digital Group I think they are great. However, they would be absolutely overwhelmed if everyone wrote or phoned with involved questions, not just because they are small but because they would probably try to answer them all. I'm convinced they will do anything reasonable, and perhaps more, to try to make you happy and to get your system going.

Are these systems for everybody? Not at all. If you want to write one check, however large, get a kit complete with every necessary nut and washer to make a finished looking piece in a slick cabinet, this is definitely not it. If you can't solder and must have consecutive detailed instructions, then make some clock kits until you gain some expertise. If you have any hardware, construction, and soldering experience and especially with a knowledgeable friend who can help then you should be able to do it. Try some of the easier boards and buy the difficult ones pre-assembled. If you've done kits before, have a suitable power supply, chassis, are determined to build your own, *and*, if money is important, then this sounds like the system for you.

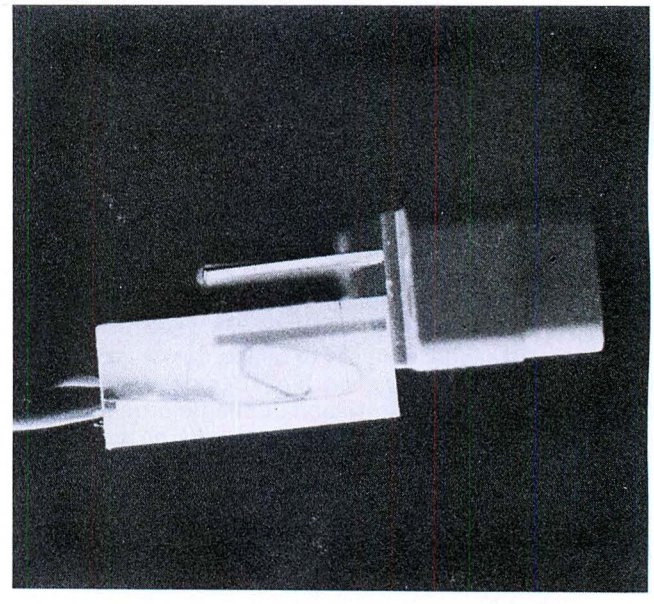


Photo 9. Special Molex Socket Shown Plugged On To Pins of a Wire Wrap P.C. Board Socket.

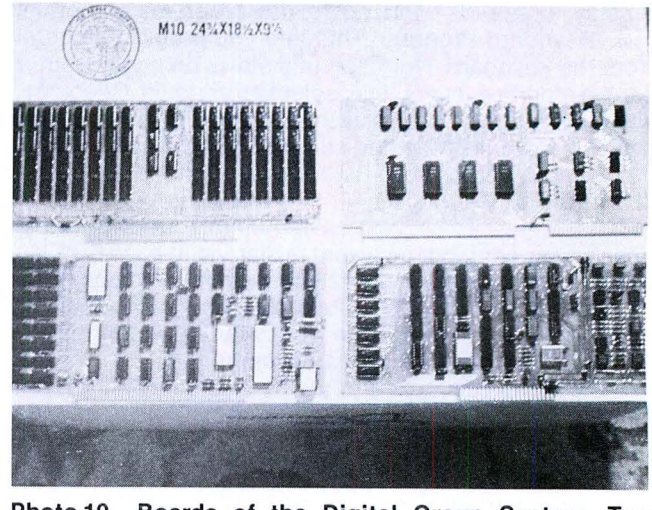
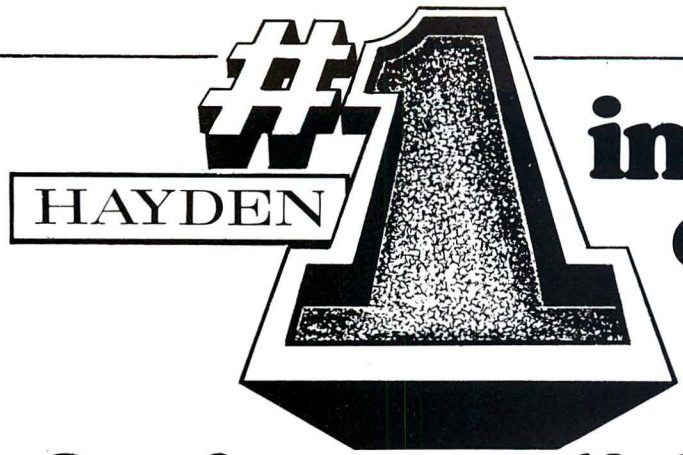


Photo 10. Boards of the Digital Group System. Top L to R—Memory, I/O. Bottom—CPU, TVC.



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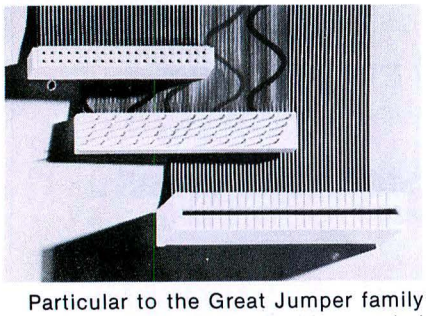
COMPONENTS

Rainbow Cabled Great Jumpers

As Great Jumpers, these are fully pre-assembled and fully pre-tested flat ribbon cable/connector assemblies. They are available in a wide variety of configurations including several line widths, a choice of conductors, and a selection of opposite end terminations.



Particular to the Great Jumper family is an especially useful double-encoded Rainbow cable. This cable is color coded line-by-line on the front, and color-striped in groups of ten on the reverse. This Rainbow cable is intended for use with single-ended Great Jumpers.

The standard cable color in the Great Jumpers family is a distinctive Electric Pink.

Double-ended and daisy-chained (Great Daisy Jumpers) configurations can include not only Card Edge Connectors, but standard double-row .100" center socket connectors and solderable printed circuit board connectors as well.

For further information, contact AP Products Inc., Box 110, 72 Corwin Drive, Painesville, Ohio 44077. (216) 354-2101.

CIRCLE INQUIRY NO. 90

EXORCISER ANALOG I/O SYSTEM

Motorola Microsystems has expanded the Micromodule Family of OEM-oriented products by adding a modular data acquisition system to the line. The system consists of an 8-channel, differential-input module called Micromodule 5A (MM5A), a 16-channel, single-ended-input module (MM5B) and a 4-channel analog output module (MM5C).

The analog input voltage range of the MM5A&B is ± 10 mV to ± 10 V; the input current range is 4 to 20 mA or 10 to 50 mA (resistor programmable). Input impedance is 100 meg Ohms; amplifier gain range is 1 to 1000 V/V (resistor programmable).

The MM5A&B both contain an input multiplexer, a high gain instrumentation amplifier, sample/hold circuit, 12 bit A/D converter, timing/control/address decode logic and a +5 V to ± 15 V dc-dc converter. Throughput accuracy is ± 0.025% Full Scale Range (± 10 V input): conversion time is 33 microseconds (± 10 V input). Sample/hold aperture time is 30 nanoseconds; common mode rejection ration (for differential inputs is 74 dB (DC to 2 KHz).

Micromodules 5A, B&C operate over a temperature range of 0°C to 70°C. Unit price of each module is $725; availability, from the factory and authorized Motorola distributors, is now.

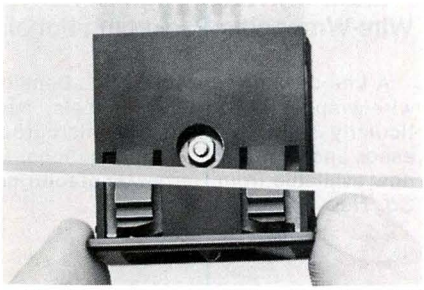
For further information, contact Motorola

Microsystems at (602) 244-6815 or the Technical Information Center, Motorola Semiconductor Products, Inc., P.O. Box 20294, Phoenix, Ariz. 85036.

CIRCLE INQUIRY NO. 91

No Tools Required To Mount New Thumbwheel Switch

New 1800 Series thumbwheel switch features front-mount, snap-in design eliminating the need for tools, panel-mounting holes, screws, nuts or washers.



The manufacturer states that the slim .315" (8mm) switch module solves panel density problems by being able to mount more switches in a smaller space.

Contacts are gold in a self-extinguishing nylon housing, with a glass epoxy circuit board. Wide variety of 10-position BCD and decimal codes available.

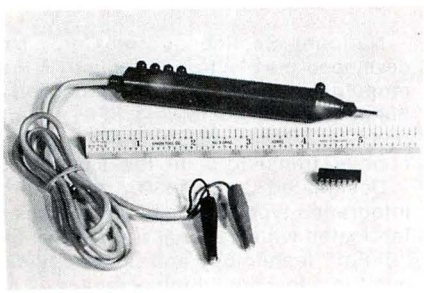
Prices start at $2 in 1,000 piece quantities, with a six week delivery for prototype units.

For further information, contact EECO, 1441 East Chestnut Ave.; Santa Ana, CA 92701 or phone "Switch Products" (714) 835-6000.

CIRCLE INQUIRY NO. 92

The Probe

A new low cost digital logic probe has been introduced by Logic Systems Inc. Probe features include: 100 Kohm input impedance, probe tip electronics protected against overvoltage, automatic pulse count memory, pulse count displayed in BCD, and counts 15ms pulses. Requires +5 volt power and works on almost any class of logic elements. The probe is assembled and tested and comes with a 90-day warranty for only $24.95. (Quantity prices available on request.)



For further information contact Logic Systems Inc., P.O. Box 7197, University Sta., Provo, Utah 84602.

CIRCLE INQUIRY NO. 93

MOSFET Transistor Improves Performance of CB Receivers

MOSFET discrete transistor designated the TIS148, the plastic packaged transistor provides 20 dB conversion gain with only a 3.2 dB conversion noise figure when used as a mixer for the 27-MHz Citizens Band equipment and eliminates the need for a RF amplifier.

A TI applications report describes the conversion of a typical bipolar tuner to use two MOSFETs with simplified circuitry, resulting in a significant reduction in third-harmonic distortion and improvement in input-overload characteristics. The report, "Dual Gate MOSFET for Citizens Band Receivers," CA-188, is available from Texas Instruments.

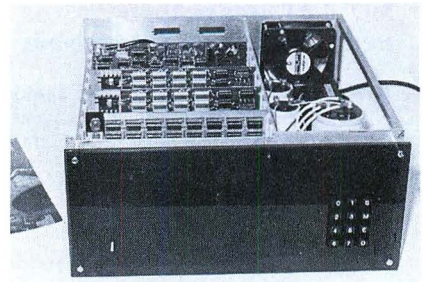
The TIS148 is priced at 30 cents each in 1,000-piece quantities and is available now.

For further information contact Texas Instruments Inc., P.O. Box 5012, Dallas, Tex.

CIRCLE INQUIRY NO. 94

S-100 Crate Design Information Package

The Objective Design Crate Information packet is a complete set of plans and specifications for building an S-100 compatible card file and power supply. The crate is of high quality, making use of standard, commercially available extrusions, card guides, and power supply components. The design is variable and can be adapted to any of the available S-100 motherboards.



The advantages of constructing a crate as opposed to buying one include: cost savings (the crate and power supply will cost approximately $150, assuming all major components are purchased in unit quantities); a sturdier crate; easier to work with design; and opportunities to meet special crate needs by customizing.

More than just a set of plans, the packet discusses:

+ The crate design and its variations
+ The crate materials—what to get, sources, substitutes, costs
+ Construction—the front panel, rear panel, support rails, etc.
+ The power supply—requirements and options, designs, parts
+ CPU and front panel options now available
+ Suggestions, ideas, customizing, etc.

For the commercial interest, the crate design can be the basis for in-house computer construction. For the hobbyist, the home constructed crate is a money-saving way to get started in personal computing.

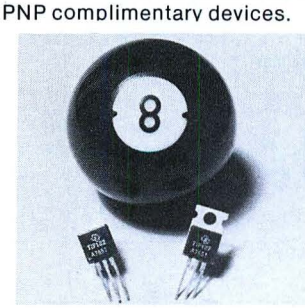
To order the S-100 crate design information packet, mail a check or money order to Objective Design, Inc., P.O. Box 20456, Tallahassee, Fla. 32304. Cost is $19.95 plus 4% sales tax for Fla. residents. Postage prepaid on all items for U.S. delivery.

For further information contact Objective Design, Inc., P.O. Box 20456, Tallahassee, Fla. 32304.

CIRCLE INQUIRY NO. 95

Plastic Darlingtons Transistors

A new series of Darlington transistors in TO220AB plastic configuration features a high current, eight ampere capability in a small plastic package, with superior power, static forward current transfer ratio, collector-emitter saturation voltage and collector cutoff current characteristics. The series is offered in NPN and PNP complimentary devices.



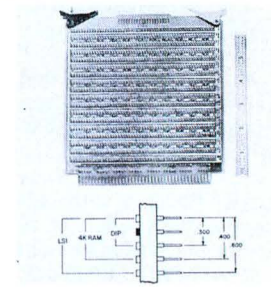
Designated TIP100, TIP101, TIP102, TIP105, TIP106 and TIP107, these Darlingtons are designed to replace 2N6045, 2N6388, MJE6045, SE9302, RCA122, 2N6042, SE9402, MJE6042, RCA8203B, and RCA126 series.

Prices for each part in 1,000 piece packages are as follows: TIP100, $.75; TIP101, $.85; TIP102, $.95; TIP105, $.85; TIP106, $.96; TIP107, $1.06.

All devices and data sheets are available now through TI and its distributors. For further information contact Texas Instruments Inc. CIRCLE INQUIRY NO. 96

Multi-Universal High-Density Wire-Wrappable Packaging Panels

A line of Multi-Universal High-Density wire-wrappable packaging panels, particularly suitable for use in microprocessor and digital-circuit applications, is now available from Garry Manufacturing Co., New Brunswick, N.J.



These universal panels will accommodate:

.100-inch spacing (SIP) Single-in-line packages; .300-inch spacing (DIP) Dual-in-line packages; .400-inch spacing (4K Ram) Memory packages; .500-inch spacing (UART); .600-inch spacing (LSI) Large Scale Integrated Circuits.

Designated the MU Series, the new packaging panels are available with 18 columns of 55 terminals per column, as plug-in modules P/N EP/80-18/55-15 or they can be manufactured to a customer's individual "slot" requirements. These panels are available in two to four weeks, at prices ranging from $1 to $1.50 per I.C. position.

For more information contact Harry A. Koppel, executive vice president, Garry Manufacturing Co., 1010 Jersey Ave., New Brunswick, N.J. 08902; telephone: (201) 545-2424. CIRCLE INQUIRY NO. 97

12-Bit Bifet A/D Building Block With P-MOS Digital Controller Chip

National Semiconductor Corp. has developed the electronics industry's first monolithic analog to digital converter building block combining j-FETs (junction-field effect transistors) and standard bi-polar transistors on the same chip.

Designated the LF13300, the ramp or integrating-type, analog building block is fabricated with National's ion implanted "Bi-Fet" technology and is the key element in a low cost, high accuracy 12 bit (plus sign) binary data acquisition system. It operates with a companion digital controller chip, the ADB1200P, built with p-channel metal oxide semiconductor

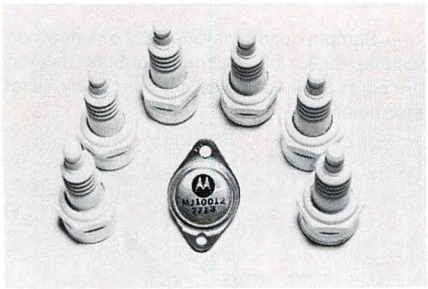
technology. In large volumes, the LF13300 chip set will sell for under $10.

For further information contact National Semiconductor, 2900 Semiconductor Drive, Santa Clara, CA 95051.

CIRCLE INQUIRY NO. 98

NEW AUTOMOTIVE DARLINGTON FROM MOTOROLA

—A new monolithic Darlington transistor circuit — type number MJ10012 — designed specifically for the high-voltage, high-current and harsh environmental requirements encountered in automotive ignition systems has been introduced by Motorola.



With a rated operating temperature range from −65° to +200°C, these new devices extend by 50° the high temperature limits of previous Darlingtons having the high energy handling capability (SOA) for the demanding automotive markets. Other specifications considered important for ignition systems have also been improved significantly, compared with similar devices previously offered by the semiconductor industry to this market.

Despite their improved specifications, the new automotive Darlingtons are priced competitively, at $2.75 in quantities of 100 to 999. The devices are available in quantity from factory and distributor stock.

For further information, contact the Technical Information Center, Motorola Semiconductor Products, Inc., P.O. Box 20924, Phoenix, Arizona 85036.

CIRCLE INQUIRY NO. 99

AMI REDUCES PRICES ON ITS FAMILY OF S6800 MICROPROCESSOR PARTS

—On the heels of a substantial reduction of the price of its S6834 4K EPROM, American Microsystems, Inc. (AMI) has announced 30 to 35 percent price reductions on the S6800 family of parts and also price reductions on the Microcomputer Development Center (MDC) and the EVK Series Prototyping Boards used in designing systems based on the S6800 microprocessor.

Price of the AMI S6800 microprocessor (an exact replacement for the Motorola M6800) is now $15.00, down from $24.00 in quantities of 100 to 999. The reduction puts the price of the S6800 microprocessor below that of the older 8080 microprocessor. Not only is the S6800 more easily programmed than the 8080, the part count (and, hence, cost) for a given system is significantly lower using the S6800 in the design.

Price reductions for other AMI S6800 family parts in 100 to 999 quantities include:

—S6820 Peripheral Interface Adapter, $6.30 (down from $10.00)

—S6810 128 x 8 RAM, $3.75 (down from $5.25)

—S6831* 2K x 8 ROM, $11.75 (down from $17.00)

AMI earlier announced a reduction in the price of its S6834 4K EPROM to $9.95 from $27.90.

AMI has also announced a price reduction for its Microcomputer Development Center from $10,500 to $9,600. The MDC is used as a software/hardware design tool. The basic price includes a "very smart" CRT terminal, dual floppy discs, a firmware de-bugger with variable formatting and disassembly features, a file-oriented operating system, an advanced screen-oriented editor, and an industry-standard assembler and loader.

Prices for the EVK Series Prototyping Boards have been reduced as well. These single-board computers range from a complete unit, factory assembled, at $715.00, to a bare PCB for classroom use at $75.00. Quantity discounts are available.

Two items of EVK software are also available on separately priced 2K ROMs; the PROTO monitor and the Micro Assembler/Disassembler. Each ROM costs $30.00.

For further information contact:
Mr. Tom Edel
American Microsystems, Inc.
3800 Homestead Road
Santa Clara, CA 95051
Telephone: (408) 246-0330

*Includes versions pin-compatible with Intel and EA ROMs.

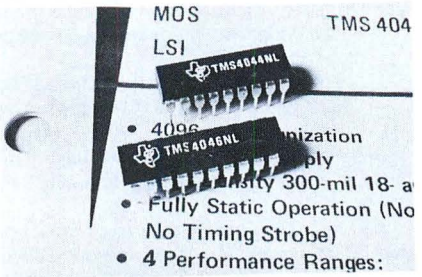
CIRCLE INQUIRY NO. 100

FOUR FULLY STATIC 4K RAM CIRCUITS

— Four new fully static random access memory (RAM) circuits have been announced by Texas Instruments. These devices now expand TI's line of NMOS 4K devices to include the largest capacity static RAMs currently available.

Types designated TMS4044 and TMS4046 are organized 4096 x 1 and types TMS4045 and TMS4047 are organized 1024 x 4. Each type comes in four speed ranges; 450, 300, 200 and 150 nanoseconds maximum access times. Since the RAMs are fully static, no clock, refresh or timing strobe inputs are reqired. All operate from single +5 volt supplies and are fully TTL compatible. A three-state output and a chip select make memory expansion simple.

Typical operating power dissipation for the 200 nanosecond versions is less than 325



milliwatts. All offer identical performance, with the TMS4046 and TMS4047 series offering an additional feature of power down operation with very low power consumption of less than 10 milliwatts. The TMS4044 and TMS-4045 are packaged in an 18-pin package; the TMS4046 and the TMS4047 in a 20-pin package.

All the RAMs have fully decoded direct addressing and are available in plastic or ceramic DIP rated over a temperature range of 0°C to 70°C.

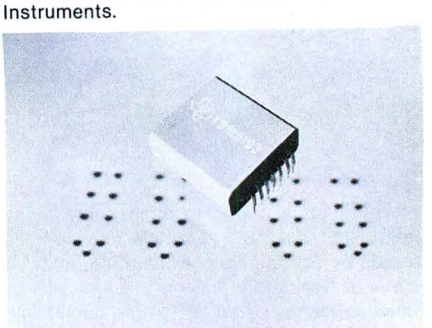
Prices in 100-piece quantities for parts in plastic DIP (with N suffix) range from $12.40 for devices with 450 nanosecond maximum access times, to $20.15 for those with 150 nanosecond access times. Prototype quantities are available now.

For further information contact Texas Instruments Inquiry Fulfillment Service, P.O. Box 1443, M/S 669 (Attn: 4K Static) Houston, Texas 77001.

CIRCLE INQUIRY NO. 101

NEW 92K-BIT MAGNETIC BUBBLE MEMORY

— Sample quantity availability of a new nonvolatile 92,304-bit magnetic bubble memory priced at $200 each was announced by Texas Instruments.



Designated the TBM0103, the device features high packing density and low access time for reliable solid-state mass storage. Modularity, provided by a single chip package, allows low entry price coupled with system packaging flexibility and efficiency.

A custom MOS controller is avaliable to provide microprocessor compatibility and a family of interface integrated circuits is in development with prototype availablity schedule for late 1977. The magnetic bubble memory system is ideally suited for portable storage.

Applications include intelligent terminals, programmable calculators, data loggers, word processing, voice storage, measurement and test equipment, and disk memory replacement in both commercial and military equipment.

The 92K-bit bubble chip is comprised of gadolinium-gallium garnet substrate upon which a magnet epitaxial film is grown. The diameter of the magnetic bubble domains is five microns. Patterns of permalloy metal are deposited on the epitaxial film to define the path of the bubble domains in the presence of a rotating magnetic field. As the field rotates, the bubble domains move under the permalloy pattern in shift register fashion.

Device architecture is major loop/minor loop. Data bits are written into and read out of the major loop; data bits are transferred to minor loops for storage. A total of 157 minor loops, each consisting of 641 bubble positions, results in a single chip memory storage capacity of 100,637 bits. However, a maximum of any 13 of the 157 minor loops on the chip is allowed to be defective. Therefore, the minimum data capacity of the remaining 144 good loops is 92,304 bits. Bubble control functions such as generate, transfer in, transfer out, replicate and annihilate are executed by providing current pulses through the appropriate control elements on the chip.

The bubble memory is packaged in a 14-pin dual-in-line module measuring 1.0x1.1x0.4 inches. The module contains a 92K-bit bubble chip surrounded by two orthogonal coils that provide the rotating magnetic field, a permanent magnet set and a magnetic shield to protect data from external fields.

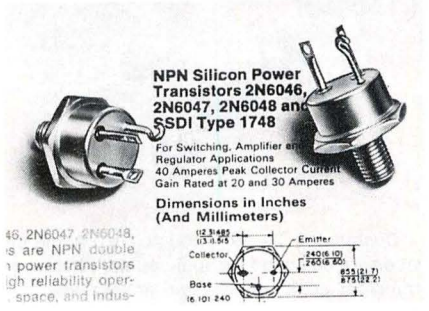
Performance specifications at 100 kilohertz operation are access time of four milliseconds for the first bit, cycle time for the 144 bit page of 12.8 milliseconds, and an approximate power consumption of one half watt for continuous operation. Operating temperature initially is 0° to 50°C with a non volatile storage range of – 40° to 85°C.

For further information contact Texas Instruments Incorporated Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: TBM0103) Dallas, Texas 75222.

CIRCLE INQUIRY NO. 102

40A POWER TRANSISTOR SWINGS UP TO 180V

—A new series of high-power NPN transistors blend a combination of high collector current, low saturation voltage, fast switching speed and high linear gain characteristics that makes them ideal for voltage-regulators, power amplifiers and switching circuits.



Designated the SSDI 2N6046, 2N6047, 2N6048 and 1748 Series by Solid State Devices, Inc., the devices have a peak collector current of 40A with V_{CEO} of 60V, 100V, 140V and 180V respectively. Maximum power dissipation is 200W at 25°C.

Maximum collector-emitter and base-emitter saturation voltage is 2V. Maximum rise time is 600 nsec and maximum fall time is 350 nsec. Direct-current gain is 100 maximum, with a typical gain bandwidth of 40MHz.

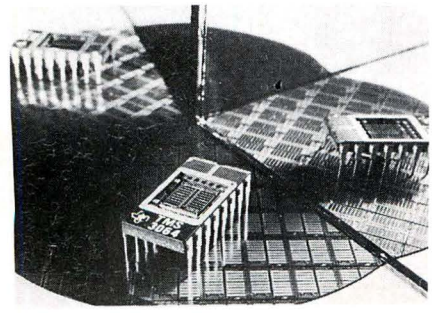
In 100 piece quantities, the devices sell for $25.00 to $40.00 each. Delivery is from stock.

For further information, contact Solid State Devices, Inc., 14830 Valley View Avenue, La Mirada, CA 90638; (213) 921-9660, TWX (910) 583-4807.

CIRCLE INQUIRY NO. 103

NEW 65K-BIT CCD MEMORY

— A new 65K-bit charge-coupled device (CCD) memory has been announced by Texas Instruments. Designated the TMS3064, the memory is organized externally as 65,536 1-bit words and internally as 16 addressable 4096-bit serial-parallel-serial (SPS) loops.



A new two-phase coplanar electrode CCD structure, developed by TI, is combined with the standard double poly N-channel silicon-gate MOS process to fabricate the device. This unique CCD structure uses ion implant storage wells allowing the simple two-phase non-overlapping clock. The two clock and the chip enable inputs can be driven by standard MOS-level drivers.

All other inputs have 200 millivolts of dc noise immunity when interfacing with standard TTL. No pull-up resistors are required. The three-state output will drive at least two standard series 74, 74S or 74LS loads without the use of pull-up resistors.

The maximum data rate is 5 mega-bits per second. Maximum access time (at 5 megahertz) is 800 microseconds. The TMS3064 has a typical operating power dissipation of 300 milliwatts at 5 megahertz and a standby power dissipation of less than 30 milliwatts. The memory comes in a 16-pin ceramic dual-in-line package with pin rows on 400-mil centers.

Designed for operation over a 0°C to 70°C temperature range the TMS3064JL has a single-piece price of $195.00.

For further information contact Texas Instruments Inquiry Answering Service, P.O. Box 1443, M/S 669 (Attn: TMS3064) Houston, Texas 77001.

CIRCLE INQUIRY NO. 104

NEW 16K-BIT EPROM

— A new 16,384-bit ultraviolet-light erasable, electrically-programmable read-only memory (EPROM) has been introduced by Texas Instruments. Designated the TMS2716, the EPROM is a direct plug-in replacement that

doubles the capacity of TI's 8,192-bit TMS2708 and TMS27L08 as well as other 2708's currently on the market, and one TMS2716 dissipates less total power than most 2708's with half the memory capacity.

The TMS2716 has the same package and pinouts, the same basic chip design and circuitry, the same power supplies and power requirements so that the new 16K-bit device may be plugged into all existing 2708 sockets.

Other TMS2716 features include

- Production proven N-channel silicon-gate technology for ready availability.
- Low power consumption, 375 mW typical.
- Guaranteed dc noise immunity in *both* high and low states so that all inputs can be driven by series 74 TTL circuits *without* use of external pull-up resistors.

The memory circuit is organized as 2048 words of 8-bit length. It is designed for high-density, fixed-memory applications where low power dissipation, fast turnarounds, and/or program changes are required. Maximum access and minimum cycle times are 450 nanoseconds. The data outputs of the TMS2716 are three-state for OR-tieing multiple devices on a common bus.

The EPROM can be erased by exposing the chip through the transparent quartz lid to high-intensity ultraviolet light. Existing PROM/EPROM programmers can be used with the TMS2716 since it has the same programming characteristics as the 2708s now in common use.

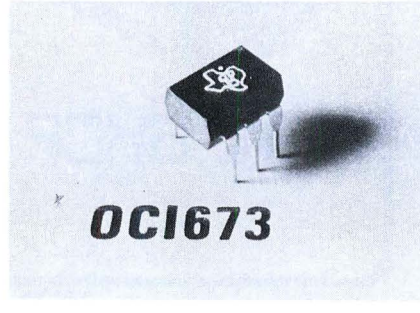
The TMS2716JL is supplied in a 24-pin dual-in-line ceramic package designed for insertion in mounting-hole rows on 600-mil centers and operates from 0°C to 70°C. It is available now at $54.75 each in 100 piece quantities.

For further information contact Texas Instruments Incorporated Inquiry Fulfillment Service, P.O. Box 1443, M/S 669 (Attn: TMS2716) Houston, Texas 77001.

CIRCLE INQUIRY NO. 105

UL LISTED ISOLATOR FOR OVEN CONTROL AND SEVERAL OTHER APPLICATIONS

— Texas Instruments Incorporated has announced a new optically coupled isolator covered by Underwriters Laboratory component recognition program and designed specifically for applications such as microwave oven controls.



Designated the OCI 673, the device is rated at 1754 volts peak and 1240 volts RMS. It is available in a 6-pin P-DIP plastic package and is a direct plug-in replacement for the TIL111 type.

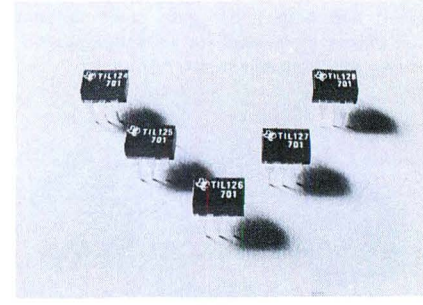
Current transfer ratio of the OCI 673 is a minimum of 25 percent. Other possible applications include open frame power supplies, industrial controls, smoke detectors, home heating and air conditioning controls, communications equipment, medical electronics and fire alarms.

The OCI 673 is available from stock and prices are $1.23 each in less than 100 quantities and $1.02 in quantities above 100 to 999.

For futher information contact Texas Instruments Incorporated Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: OCI673) Dallas, Texas 75222. CIRCLE INQUIRY NO. 106

FIVE HIGH VOLTAGE ISOLATORS

— A series of five high-voltage, optically coupled isolators rated at 5KV isolation voltage has been introduced by Texas Instruments Incorporated.



Designated TIL124 through TIL128, the devices are designed for applications where high transient peak voltages are encountered and where added isolation protection is desired.

The isolators are available in two configurations. Three of them provide transistor output with minimum current transfer ratio of 10, 20 or 50 percent. The other two offer Darlington connections with minimum CTR of 300 percent.

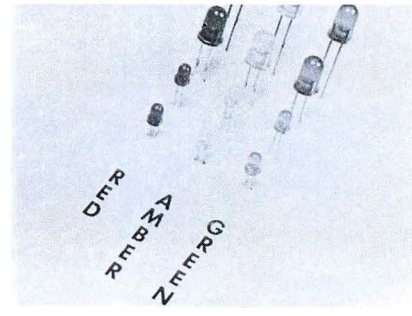
Applications include power supplies, telephone circuits, relay and pulse transformer replacements, machine tool controls and CB radio transmitters.

All types are compatible with TTL logic and are available in 6-pin plastic DIP packages. The series can be interchanged, both electrically and mechanically, with the TIL111 family as well as with other types.

For further information contact Texas Instruments Incorporated Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: TIL124-TIL128) Dallas, Texas 75222. CIRCLE INQUIRY NO. 107

NEW HIGH-INTENSITY VLED SERIES

—A new series of high-intensity, gallium phosphide visible light-emitting diodes (VLEDs) has been introduced by Texas Instruments.



Two sizes are available in red, amber or green. The small T-1 diameter size VLEDs are designated TIL212 (amber), TIL216 (red) and TIL232 (green). The larger T-1-¾ diameter size devices are designated TIL224 (amber), TIL228 (red) and TIL234 (green).

The VLEDs in molded epoxy packages are direct replacements for many other types currently being used. They feature brightness outputs of up to 25 microcandelas at 50 milliamperes, low power consumption and long life.

The devices are ideal for such applications as battery operated apparatus, array lighting, backlighted panels, microprocessors, incandescent lamp replacements, diagnostics, indicator lamps and instrumentation panels and others requiring low cost, high intensity VLEDs.

The T-1 diameter size devices are offered at $.58 each in under 100-quantities and $.46 for up to 1,000 pieces. The T-1-¾ diameter size VLEDs are priced at $.62 each in under 100 quantities and $.49 for up to 1,000.

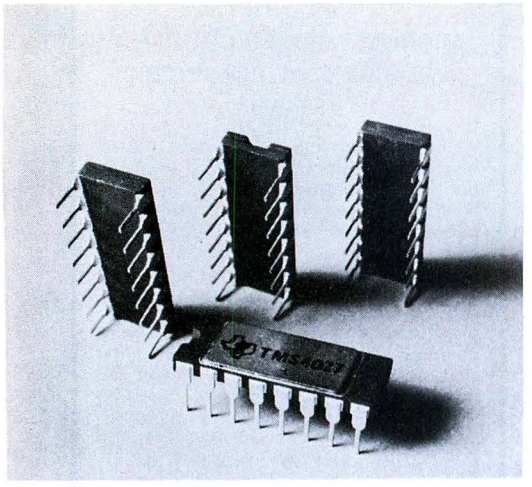
For further information contact Texas Instruments Incorporated Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: TIL212-234) Dallas, Texas 75222.

CIRCLE INQUIRY NO. 108

NEW, HIGH-PERFORMANCE 4K 16-PIN DYNAMIC RAM

— A new, high-performance 4096-bit, 16-pin dynamic RAM has been introduced by Texas Instruments. This expands TI's line of dynamic memories to 14 devices, making TI the only supplier to offer 4K dynamic RAMs in 16,18 and 22-pin versions.

Designated the TMS4027, the new RAM features:



- 150 nanosecond access time, 320 nanosecond cycle time.
- ±10% power supply tolerance (+12V, ±5V).
- Low power 460 mW active, 27 mW standby (maximum).
- Common I/O capability.
- Gated RAS, RAS-only refresh, and page-mode capability.
- Inputs are TTL compatible with low capacitance.
- 16-pin space-saving dual-in-line package.
- Input latches for addresses, chip select, and data in.
- Three-state TTL-compatible high-drive outputs.
- Output data latched and valid into next cycle.

The TMS4027 is a 4096 word by 1 bid MOS random access memory fabricated with TI's N-channel silicon-gate process. TI's TMS4027 uses a single transistor storage cell with new dynamic storage and control circuits, achieving high performance and low power dissipation.

The mulitplexing/latching of address inputs allows the TMS4027 to be packaged in a 16-pin 300 mil-pin-row DIP, reducing memory board space requirements by 40 percent over 22-pin packages.

System advantages of using the TMS4027 include: direct interfacing with TTL, elimination of external interface register, reduction of address lines to only six low-capacity lines, increased noise immunity, and a choice of two chip-select methods, and the ability to add read-modify-write page mode, or RAS only refresh modes.

The TMS4027 is offered in a 16-pin dual-in-line package designed for insertion in 300 mil mounting-hole row centers. It operates from 0° to 70°C. Prototype quantities are now available. The TMS4027 is priced at $19.20 in 100 piece quantities.

For further information contact Texas Instruments Incorporated Inquiry Fulfillment Service, P.O. Box 1443, M/S 669 (Attn: TMS-4027) Houston, Texas 77001.

CIRCLE INQUIRY NO. 109

Single-Chip Microprocessor Controller

The MC10801 Microprogram Control Function is a bipolar LSI circuit, a member of the M10800 MECL Processor Family which controls the sequence of the microprogram instructions stored in a processor's control memory. The MC10801 responds to a set of 16 powerful jump and branch instructions. Mnemonic labels for each of the instructions simplify microprogram development by expressing program flow in easy-to-use assembly level language format. While designed for the M10800 Processor Family, the MC10801 is also useful as the microprogram controller in a MECL 10,000 system.

For further information contact Bi-Polar Marketing at (602) 962-2151 or the Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20294, Phoenix, AZ 85036.

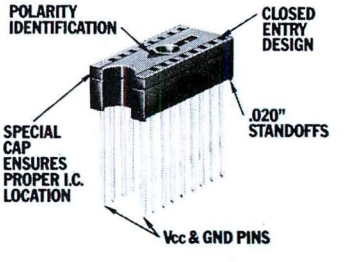
* Trademark of Motorola Inc.

CIRCLE INQUIRY NO. 110

16-Pin Discrete Wrap Sockets

A unique 16-pin discrete arrangement saves labor, time, and machine costs by eliminating the need for mounting separate power and ground pins into the board. The new socket contains two additional dummy pins for commitment to Vcc and GND, and also has a specially designed cap that ensures proper insertion and location of 16-pin DIP devices.

Depending on how a particular I.C. socket board is configured, many significant savings can be realized through use of the 16-Pin Discrete. The socket need only be plugged into the board as the power and ground pins are provided as part of the socket unit. A patent has been applied for on the design of the Discrete socket.



XIMEDIA PRESENTS

The SOROC IQ120

CURSOR CONTROL. Forespace, backspace, up, down, new line, return, home, tab, PLUS ABSOLUTE CURSOR ADDRESSING.

TRANSMISSION MODES. Conversation (half and full Duplex) PLUS BLOCK MODE — transmit a page at a time.

FIELD PROTECTION. Any part of the display can be "protected" to prevent overtyping. Protected fields are displayed at reduced intensity.

EDITING. Clear screen, typeover, absolute cursor addressing, erase to end of page, erase to end of line, erase to end of field.

DISPLAY FORMAT. 24 lines by 80 characters (1,920 characters).

CHARACTER SET. 96 characters total. Upper and lower case ASCII.

KEYBOARD. 73 keys including numeric key pad.

REPEAT KEY. 15 cps repeat action.

DATA RATES. Thumbwheel selectable from 75 to 19,200 baud.

SCREEN. 12 inch rectangular CRT — P4 phosphor.

SPECIAL INTRODUCTORY PRICING

Kit $ 995.00 **Assembled $ 1,295.00**

(Price includes block mode, lower case and 24 line options.)

IMSAI + Z-80

XIMEDIA is offering a special price on an IMSAI I-8080 with a TDL ZPU Z-80 board instead of the standard 8080 cpu.

The system includes:
IMSAI I-8080 without cpu board. 22 slot mother board with 22 *pre-soldered* connectors and card guides; cooling fan.

Price:

Kit	Assembled
$ 999.00	$ 1,295.00

Selectric Terminals $1,200.00

AT LAST!

An ASCII coded Selectric terminal with a RS232-C interface.

Call or write us today for details.

XIMEDIA OFFERS A FULL RANGE OF PRODUCTS FOR THE PERSONAL COMPUTER ENTHUSIAST AND THE SMALL SYSTEM DESIGNER. LET US QUOTE ON ALL YOUR HARDWARE AND SOFTWARE NEEDS.

OUR RETAIL STORE — THE COMPUTERIST™ — IS NOW OPEN IN SAN FRANCISCO. CALL US FOR DIRECTIONS.

XIMEDIA

1290 24th Avenue • San Francisco, CA 94122

(415) 566-7472. Please call collect!

California residents add 6% sales tax. Please allow 3 weeks for delivery.

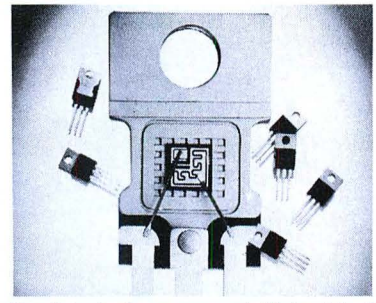
The 16-Pin Discrete has proven so successful in cost savings that Scanbe itself has taken advantage of the new concept by introducing several new 16-pin socket cards and panels, and is passing the savings gained by using the new sockets on to its customers. Typical pricing of the sockets is 39 cents each in lots of 1000.

For further information contact Scanbe Marketing Services, a Division of Zero Mfg. Co., 3445 Fletcher Avenue, El Monte, CA 91731; (213) 579-2300.

CIRCLE INQUIRY NO. 111

Motorola to "Alternate-Source" Popular Plastic Power Transistors

Motorola has supplemented its extensive line of plastic-packaged power transistors with a series of 20 new devices that duplicate the more popular TI and RCA-registered devices. Included in the new offering by Motorola are six Darlington devices and 14 discrete transistors in the 65 Watt power category. These devices are being introduced at prices that are 5 to 10 percent below published competitive prices at the time of introduction.



The introductions represent Motorola's first use of the TO-220 plastic package for silicon power transistors. This is in addition to the plastic cases, 77, 90 and 199 which have housed the company's plastic power line up to now. Customers however can continue to purchase devices with similar electrical specifications in the other Motorola plastic packages.

Motorola plans to extend its use of the TO-220 package to other power device types as quickly as production capability permits.

Product availability is now, from the factory and from authorized Motorola distributors.

For further information contact Silicon Power Marketing at (602) 244-4284 or the Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20294, Phoenix, AZ 85036.

CIRCLE INQUIRY NO. 112

8,192-Bit UV Light Erasable Programmable Read-Only Memory

The TMS 2708JL, is pin-for-pin compatible with the Intel device with the same part number.

Maximum access and minimum cycle times are 450 nanoseconds. The 184 x 124 mil chip is more than 11 percent smaller than the Intel chip, potentially allowing improved manufacturing productivity.

This smaller chip size is due to TI's unique periphery circuit design techniques which also reduce power consumed by the TMS 2708. Typical power dissipation is less than 450 milliwatts.

The memory circuit is organized as 1,024 words of 8-bit length. It is designed for high-density, fixed-memory applications where fast turnarounds and/or program changes are required.

The device is fabricated using an N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs can be driven by Series 74 TTL circuit without external resistors.

The data outputs are three-state for OR-tieing multiple devices on a common bus. A pin-compatible mask programmed ROM, the TMS4700, is available for large volume systems.

The EPROM can be erased by exposing the chip through the transparent lid to high-intensity ultraviolet light at a recommended exposure of 10-watts-seconds per square centimeter.

The TMS2708 is supplied in 24-pin dual-in-line ceramic packages designed for insertion in mounting-hole rows on 600-mil centers and operates from 0°C to 70°C.

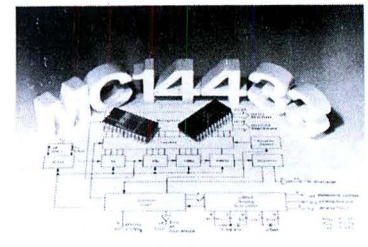
Prices for each part are as follows: 1-24, $98.00; 25-99, $73.00; 100+, $64.00. Parts are available now.

For further information contact Texas Instruments Incorporated, Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: TMS 2708), Dallas, TX 75222; (713) 494-5115, Ext. 3281.

CIRCLE INQUIRY NO. 113

Low Cost 3½ Digit CMOS A to D Circuit

A new single-chip CMOS integrated Circuit that requires only two external resistors and two capacitors and a single voltage reference to form a modified, dual-slope, analog-to-digital converter is now available from Motorola. It is designed for DVM/DMM, digital thermometer, digital scale applications, and can be used in MPU systems. The 3½ digit circuit, designated the MC14433, has a multiplexed BCD output format and has an intrinsic full scale range of ±199.9 mV (200 mV reference) or ±1.999 V (2 V reference), with an input impedance of more than 1000 megohms. The MC14433 dissipates very little power, typically 8 mW for ± 5 volt supplies. This unit operates well with both LED and LCD displays.



Other features include: ±0.05% of reading accuracy; Up to 25 conversions per second; Autopolarity; Auto Zero; Standard B-Series outputs; On-chip or external clock; Overange and underange signals. The MC14433 uses the techniques developed by Motorola to put both linear and digital functions on one chip. The linear functions contained are high-performance, low-power operational and differential amplifiers.

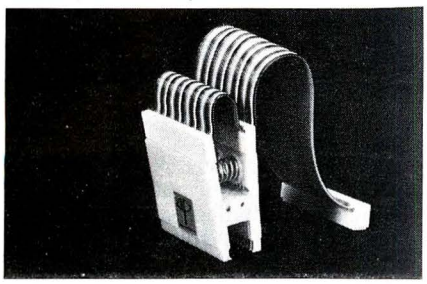
The MC14433 package is a 24-pin dual-in-line in either plastic ("P" suffix) or ceramic ("L" suffix). Pricing in quantities of 100 to 999 is $9.97 for the MC13322P and $14.95 for the MC14433L. Availability is off-the-shelf from the factory or distributor stock.

For further information contact Technical Communications, Motorola Integrated Circuit Division, 3501 Ed Bluestein Blvd., Austin, TX 78721.

CIRCLE INQUIRY NO. 114

The Logical Connection

The Logical Connection is a special version of AP's popular Great Jumpers. Like Great Jumpers, The Logical Connection comes fully pre-assembled and fully pre-tested with molded-on connectors that feature integral strain relief and line-by-line *probeability.*



The Logical Connection DIP ICs are designed to mate directly with the contact posts of AP's IC Test Clips. These IC Test Clips, first developed by AP a decade ago, provide pin-by-pin connection to DIP ICs. Their contact comb assembly safeguards against accidental misplacement or shorts. And the IC Test Clips are steel coil spring-loaded for a sure, reliable grip.

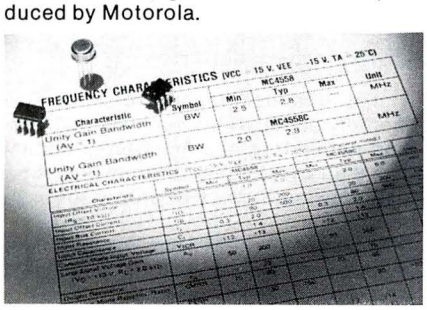
The Logical Connection translates the pins atop AP's IC Test Clip into a standard double row flat cable socket connector through any desired length of Great Jumpers ribbon cable.

For further information, contact AP Products Inc., Box 110, 72 Corwin Drive, Painesville, Ohio 44077, (216) 354-2101.

CIRCLE INQUIRY NO. 115

OP AMP Triples Frequency Range

A dual operational amplifier with the characteristics and package options compatible with the "industry standard" MC1558/MC1458, but *with nearly three times its unity-gain bandwidth* is produced by Motorola.



Designated *MC4558/MC4558C,* the new devices can be plugged directly into sockets of existing designs, currently using MC1558/1458 types, in order to expand the unity-gain bandwidth of the circuits from 1 MHz to 2.8 MHz without affecting other characteristics. They are ideal for new designs whose required bandwidth previously prohibited the use of low-cost operational amplifiers, and are available in quantity from Motorola warehouse or all distributors.

For further information, contact Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, Ariz. 85036. Phone 244-6900. CIRCLE INQUIRY NO. 116

EQUIPMENT

Portable Universal Programmer

The Data I/O Model 9 is a highly versatile, software based PROM programmer in a compact lightweight package. It features insert/delete data editing capabilities and is capable of programming, loading, and verifying more than 200 different PROM configurations. It can program entire generic PROM families using a single personality module.

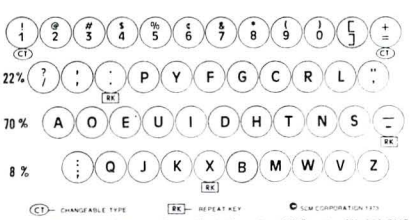
Model 9 features hexadecimal keyboard and display. All operations are microprocessor controlled, resulting in extremely simple operation. Software based serial and parallel I/O interfaces allow for data communication in key-selectable data translation formats. Data polarity controls are provided, and built-in error checking routines assure the accuracy of all data transfers. The integral 1K-byte RAM buffer memory is expandable to 4K-byte capacity, allowing use of the programmer with larger PROMs of the future.

Capable of interfacing with the Data I/O Ram-Pak, Model 9 emulates PROMs of any configuration, and may also be used as a portable secondary RAM buffer if desired. It is lightweight and portable (17 lbs.) and measuring 11" x 6" x 15". A 1K RAM buffer memory isstandard; I/O interfaces, Ram-Pak Interface, and carrying case are optional. Base price is $1975. Program card sets, including generics, cost $400. Delivery in 45 days.

For more information, contact Data I/O Corp., 1297 Northwest Mall, Issaquah, Washington 98027. Phone: (206) 455-3990. Telex: 320290. CIRCLE INQUIRY NO. 117

Simplified Keyboard

Anyone getting into computer work who doesn't type should study the Dvorak Simplified Keyboard. It's learned in third the time and is twice as productive. Big corporations are studying its use but until the schools teach it, they can't get operators without re-training school graduates from the standard board training.



The individual with his own set-up can get input units with any kind of board desired. A number of software companies

are working to provide DSK or ASK, (American Simplified Keyboard, an SCM variant) for study. Eventually all alpha input will be by means of this arrangement.

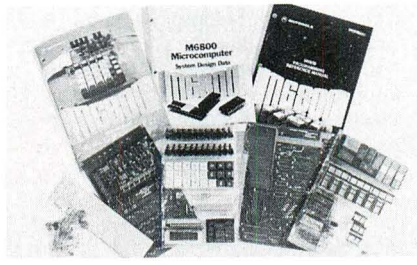
The standard board is left-handed, four fingered, and 28% of the strokes are one-handed between rows, the slowest and most difficult of strokes. Actual time spent in typing on the standard board is less than half, the rest is travel between rows in one hand or the other. Dvorak's change cut the travel by 86%, automatically nearly doubles productivity just by reducing travel time.

For further information contact 3 Readiness Society, Inc., 6755 W. Broward #201, Plantation, FL 3317, 305-583-2419.

CIRCLE INQUIRY NO. 118

M6800 Microcomputer Kit

A microcomputer evaluation kit for M6800 systems is now available from the Integrated Circuit Division of Motorola Inc.



The kit, MEK6800D2, when assembled, is a fully functional microcomputer system based on the MC6800 microprocessing unit and its family of associated memory and I/O devices. It is made up of two basic units, a Microcomputer Module (9.75″ × 8.3″), and a Keyboard/Display module (10″ × 6.25″) the latter containing audio cassette interface circuitry (Kansas City Standard).

The display consists of six, seven-segment LED readouts that display address (four units) and data (two units) in hexadecimal format. The keyboard is hexadecimal with eight additional command keys.

Also included in the kit three-ring binder is an assembly manual that covers testing, schematics, monitor program listing and parts listing. An M6800 Programming Reference Manual and the M6800 Microcomputer System Design Data book are also part of this package. The kit may be used "as is" or expanded to a full 65K system.

Cost of the kit is $235.00 (power supply (5 volts at 2A) and cassette recorder not included), and is available from Motorola Distributors.

For further information contact Motorola Semiconductor Products, Inc., 3501 Ed Bluestein Boulevard, Austin, Tex. 78721, (512) 928-2600.

CIRCLE INQUIRY NO. 119

32K Bit Fully Static MOS ROM

A 32,768 bit fully-static MOS Read Only Memory, designated the TMS 4732, is organized as 4096 words of 8-bit length and is fabricated with N-Channel Silicon-Gate Technology.

It is intended for high-density, fixed memory applications such as logic function generators and microprogramming. The 8-bit byte organization makes it particularly useful in microprocessor-based systems.

Maximum Access Time is 450 ns, Minimum Cycle Time is 450 ns, and typical power dissipation is 450 mW.

The TMS 4732 is fully TTL compatible as all inputs can be driven directly by series 74 TTL circuits without the use of external pull-up resistors, and each output can drive two series 74 TTL circuits without the use of external resistors. All data outputs are three-state for OR-Tieing multiple devices to a common bus.

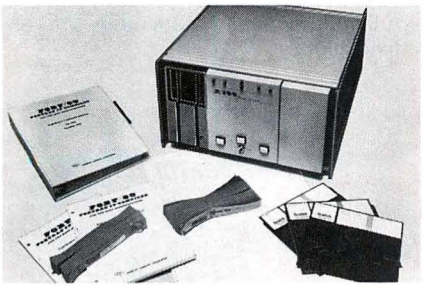
Designed for operation over a 0° to 70°C temperature range, the TMS 4732 sells for $20.00 each in quantities of 1000 pieces.

For further information contact Texas Instruments Inc., Inquiry Answering Service, P.O. Box 5012, M/S 308 (Attn: TMS 4732), Dallas, Tex. 75222.

CIRCLE INQUIRY NO. 120

Z//100 Series of Portable Microcomputer Systems

"The Personal FORTRAN Machines" are three machines in the Z//100 series are the first low-priced portable 8080-based microcomputer systems to be offered complete with a file management system and FORTRAN IV Compiler.



All three models in the new family are built around an 8080 CPU and include 3K of PROM and a minimum of 33K bytes of RAM, expandable to 64K. The systems include an IBM compatible dual diskette drive, offering 512 Kbytes of on-line storage. A second dual drive can be mounted in the table-top cabinet for a system total of 1 megabyte of on-line storage. The diskette drives feature voice coil positioning and motorized loading and unloading of diskettes.

The Z//100 systems are available with a monitor, a complete file management system and FORT//80, RCC's previously announced 8080 resident FORTRAN IV compiler. FORT//80 is a subset of ANSI FORTRAN IV, producing directly executable optimized 8080 machine code. FORT//80 (including IBM format floating point) requires 11K of memory. It includes a number of powerful language extensions which allow the user to take maximum advantage of the 8080 hardware. These include program control over interrupts and 8080 flags, direct FORTRAN addressing of 8080 ports, and the ability to link inline machine code into a FORTRAN program. Prices range from $7,995 for Z//100-1, $8,995 for Z//100-2 and $9,795 for Z//100-3.

The FORTRAN compiler, FORT//80, is available with any of the Z//100 configurations, priced at $750.

Delivery is 30 days ARO.

For further information, contact Realistic Controls Corp., 3530 Warrensville Center Rd., Cleveland, Ohio, 44122.

CIRCLE INQUIRY NO. 121

Computer Music With The SB1 Music Board

The SBI Music Board is S100 bus computer compatible and can generate complex wave forms because attack and sustain reside in hardware, not software, as in previous alpha-numeric systems developed. Plus, a new high level music language developed for the system allows the user to input music notes via keyboard with ease. The envelope, frequency (tone), 16 levels of volume and 9 octave levels are all software selectable.

There is a two-pin connector in the card that plugs into a regular audio system. The SB1 can generate realistic sounds of most instruments and with additional boards, it can play a variety of notes from a variety of instruments creating a symphonic atmosphere. Accuracy is said to be better than ½ % for one octave of the tempered scale.

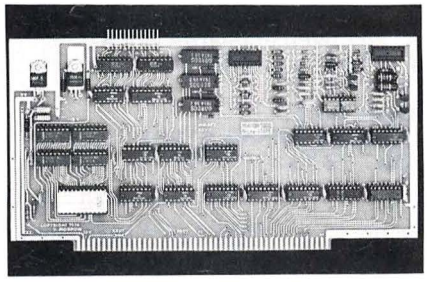
The SB1 will be offered through computer hobby stores, or directly, and can be heard at the First West Coast Computer Faire in San Francisco, April 16 to 17. Prices for the SB1 are $250 in kit form, and $300 fully assembled and tested. All kits include full documentation and assembly instructions. Software is also included.

For further information, contact Cybercom, a Division of Solid State Music, located at 2102A Walsh Avenue, Santa Clara, CA 95050. Telephone (408) 246-2707.

CIRCLE INQUIRY NO. 122

Combined Cassette Interface — I/O Board

Fully compatible with the S-100 buss and "Kansas City" standard data format, this board links your computer to three inexpensive audio cassette machines for mass memory applications (including sort and merge operations).



A serial port allows simultaneous communication with a Teletype incorporating reader control, as well as any RS-232 serial device (such as a Modem or video terminal); a general purpose, 8 bit parallel port with handshaking signals accomodates such devices as an ASCII keyboard or tape reader. The board carries firmware in ½ Kbyte of PROM, which stores all routines needed for cassette interfacing, UART simulation, and data transfer between the microcomputer's memory and the ½ Kbyte of onboard RAM.

Buffers isolate internal data paths from the buss; onboard regulation simplifies power requirements. Available both in kit form ($120) and assembled/tested/warranted ($165) by mail or from many computer stores. Includes documentation. Available from stock.

For further information contact Morrow's Micro-Stuff, Box 6194, Albany, CA 94706.

CIRCLE INQUIRY NO. 123

Versatility and Control Are Keys in the Software Controlled Video Board Cybercom/Solid State Music

Video Board called the VBI, is plug-in compatible with S-100 bus systems such as Altair and IMSAI computers. VBI is the first complete software-oriented video system available offering more versatility

and exceptional control to the user. The cursor, video reverse, and graphics are software-controlled with no internal hardware adjustments necessary for various operational changes.

Other features of the VBI include on-board dip switch selection of 32 or 64 characters per line, with 16 display lines; upper and lower case and Greek alphabet with other interchangeable fonts readily available; 2 × 3 matrix graphics; parallel and composite video outputs to video monitor or TV set; and, the VBI can be addressed for any 1K block of memory.

The VBI will be offered in kit or assembled form. Price in quantity of one is $189.95 in kit form, and $269.95 assembled and fully tested.

For further information contact Cybercom, a Division of Solid State Music, located at 2102A Walsh Ave., Santa Clara, CA 95050. Telephone (408) 246-2707.

CIRCLE INQUIRY NO. 124

Micromodule 6—A 2K-Byte Static RAM Module

Micromodule 6™, designated M68MM06, provides the user with 2048 bytes of static RAM (type P2102-1 or MK4102 RAMs are used as the memory elements), organized into two groups of eight 1024 X1 bit RAMs. Typical memory cycle time is 500 nanoseconds.

During manufacture, Micromodule 6 is assigned to base address 7800 (hex) to 7FFF (hex). The user, however, can change this base address by means of jumper wires on the module. The base address can be re-assigned throughout the range of 0000 to F800, in 2K byte increments. The Micromodule's address, data and control busses have TTL-compatible buffered inputs; the data bus has three-state TTL outputs. M68MM06 is bus compatible with both the Micromodule Family and the EXORciser™. This adaptability permits the user to utilize the hardware and software features of the EXORciser and its options to aid in system development and production line troubleshooting.

Power requirements for Micromodule 6 is 1.5 A (max) at + 5 Vdc (± 5%). Operating temperature range is 0°C to 70°C. The unit price is $280; the 2 to 9 price is $274. Availability, from the factory and authorized Motorola distributors, is now.

For further information contact Motorola Semiconductor Products, Inc., P.O. Box 20924, Phoenix, Ariz. 85036.

CIRCLE INQUIRY NO. 125

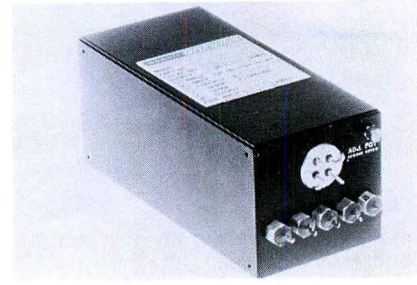
Three New Keyboard Cases

E., S. & L., Industries produce three new keyboard cases for the Controls Research Corporation Keyboard #53A-013000-C. The cases are 14" wide, 3-1/4" high and come in three depths: 7", 8-1/2" and 10-1/2".

For further information contact E.S. & L. Industries, Inc., Post Office Box 1260 E. Southgate CA 90280, (714) 956-1477, (213) 566-1677.

New Power Module

Abbott has designed a new high efficiency series of dual output power modules that convert 28 VDC input power to 25, 50, or 100 watts of regulated DC power at plus and minus 15 volts. The new BBN-15A Series is one of the few switching regulated power supplies capable of operating over the full military temperature range of – 55°C to + 100°C.



The BBN-15A Series regulates DC input voltages to 0.5% over its full input range of 20 to 32 VDC. Load regulation is 0.5% for no load to full load at constant input voltage. PARD (ripple and noise) has been reduced to 25 mV RMS, 100 mV peak-to-peak over the temperature range of 25°C to 100°C. Other features include full rated output current over the temperature range of — 55°C to 85°C, derated to 80% of full load rating at 100°C (baseplate temperature). Temperature Effect (co-efficient is specified at 0.03% per degree Celcius.

Abbott's BBN-15A Series of power modules are completely protected against short circuits of any duration, and will withstand an input voltage transient of 80 VDC for 0.1 second. Internal overvoltage protection is available as a low cost option, with a built-in delay of approximately 500 microseconds to minimize "nuisance" tripping.

Prices are: 25 watt, 1-4 Pcs., $325; 50 watt, 1-4 Pcs., $375; 100 watt, 1-4 Pcs., $450. Quantity discounts are available for large orders.

Delivery is within 10 weeks after receipt of order.

For further information contact Abbott Transistor Labs., Inc., 5200 W. Jefferson Blvd., Los Angeles, CA 90016. Telephone (213) 936-8185, Telex 69-1398.

CIRCLE INQUIRY NO. 126

Selectable Baud Rate RS-232 Compatible Output Table-Top Mount ASCII Keyboard

The versatile GCT-3071 table-top mount ASCII code RS-232 output compatible keyboard features selectable baud rates ranging from 110Hz to 19.2KHz—an exclusive.

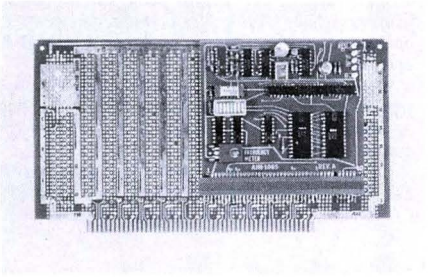
It also has a full interactive 16-lighted pushbutton switch array that allows the input of up to 64 different programming functions. Other features include: a high speed entry pad, automatic repeat on all keys, two-key roll-over with N-key lockout, five cursor control keys, and selectable parity (ODD, EVEN or NONE). It has 128 ASCII characters. Completely contained in a compact, low profile housing, the GCT-3071 is single unit priced at $1,500.

Contact William Huber for further details. Genisco Computers, 17805-D Sky Park Circle Drive, Irvine, CA 92714. Phone: (714) 556-4916.

CIRCLE INQUIRY NO. 127

AIM-1005 Frequency Meter

Automated Industrial Measurements (AIM) has announced a frequency meter, AIM-1005, that may be directly interfaced with 8-bit microcomputers. It has 13 bits of resolution plus overrange, and has eleven time-base ranges, from 10 μ seconds to one hour.



AIM-1005 is interfaced with the microcomputer as if it were memory, and can be located in 14 different locations. These locations are controlled with switches on the board as is the time-base range. It is accurate to within ± 1 count over the entire operating temperature range of 0°C to 70°C. The input frequency range is from DC to 25 MHz minimum. The input can be TTL, or the input comparator may be used which provides ± 15 volts of common mode as well as a high impedance input. An optional input is an AIM-1003, which allows one of AIM's transducer digitizers to be connected using only a twisted pair of wires. The input connections can be made from standoffs on the top of the board, or through the edge connector.

The complete frequency meter is on a 4″ by 4½″ printed circuit card with a 40-pin edge connector with contacts on 0.1″ centers. Because of its compact size, AIM-1005 is available mounted as a daughter board on the larger microcomputer cards, such as the Altair or IMSAI. Such a desirable option is offered by AIM for merely $30 additional. AIM-1005 will also fit into any 4½″ card cage system, such as the Zilog Z80 or the Pro-Log systems.

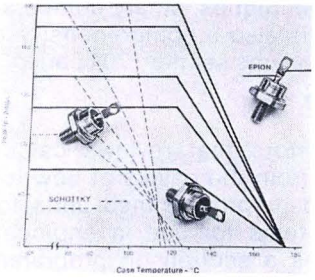
AIM-1005 is priced at $178 each in quantities of 1-9, and is available from stock.

For more information contact Barry Hilton, Automated Industrial Measurements Inc., P.O. Box 125, Wayland, Mass. 01778. Tel: (617) 653-8602.

CIRCLE INQUIRY NO. 128

Ion-Implanted Diodes Replace Schottkys

Two new ion-implanted diodes, provide the fast switching and low forward voltage associated with Schottky diodes while exhibiting substantially better temperature characteristics, reverse leakage currents and an order-of-magnitude lower junction capacitance.



Designated the 1N6097E and 1N6098E, the device characteristics give significant efficiency improvement and reduced component count in conventional and switching power supplies to 100KHz. The E designator signifies that the diodes are manufactured with SSDI's proprietary EPION® ion-implantation process.

The 1N6097E and 1N6098E have an average half-wave rectified forward current of 50A with a dc blocking voltage of 30V and 40V respectively. Both devices have a maximum forward voltage of 0.86V. The SSDI ion-implantation technique produces a maximum reverse recovery time of 75 nanoseconds with 50 nanoseconds typical. This is in the same range as the Schottky; however, since Schottky is a majority carrier device, it is difficult to measure actual recovery time independent from circuit affects.

The 1N6097E is priced at $11.25 each in 100 piece quantities; the 1N6098E is priced at $13.90 each in 100 piece quantities. Delivery is stock to 4 weeks.

For further information contact Solid State Devices, Inc., 14830 Valley View Ave., La Mirada, CA. 90638; (213) 921-9660; TWX (910) 583-4807.

CIRCLE INQUIRY NO. 129

SOFTWARE

Simple, Easy-To-Use, High-Level Language For SC/MP Microprocessor Systems

A new, simple, easy-to-use microcomputer language, similar to BASIC, has been developed by National Semiconductor Corp. for use with its popular 8-bit SC/MP microprocessor system.

Called NIBL (pronounced "nibble") for National Industrial Basic Language, this microprocessor programming aid is aimed at making th SC/MP as easy to use as possible for those trained neither in electronics nor computer programming. To insure the widest possible dissemination of the SC/MP-oriented NIBL, says Phil Roybal, microprocessor product marketing manager, it has been placed, without

charge, in the public domain. It is available in paper tape form through COMPUTE, the National Semiconductor Microprocessor Users Group newsletter. In preparation is a new self-teaching manual for NIBL and the SC/MP LCDS (low cost development system), and a soon-to-be-released NIBL firmware package in read-only memory.

For further information contact National Semiconductor, 2900 Semiconductor Drive, Santa Clara, CA 95051, Telephone (408) 737-5000 TWX: 910-339-9240, Cable NATSEMICON, Telex: 346353.

CIRCLE INQUIRY NO. 130

Time-Sharing-Service Supports Business-Use of Micro-Systems

Quikdata Timesharing Service is now operating over (213) & (714) datalines at 110/300/1200 bauds. Its unique features are free program use for many commercial and engineering applications, written in business basic and table-driven. Changes in logic and I/O formats are easily implemented mostly without reprogramming. Remote job entry, spooling, free format, batch data editor are standard options. Remote users will find the service most economical because data files can be polled during the night and processed for printout from cassette or floppy disc next morning. It is a cost efficient extension of microprocessors for large volume EDP-tasks using 1200 baud dial-up telephone lines. Typical phone-charges coast to coast are 1 cent/600 bytes between 23:00 to 8:00 and on weekends.

Minimum configuration requires basic language with I/O control for cassette or floppy disk and originate modem; next phase uses polling according to protocol in basic.

For further information contact Quikdata, c/o Ernest J. Schubert, 3431 Cerritos, Los Alamitos, CA 90720. CIRCLE INQUIRY NO. 131

Text Editing System

TSC announced the availability of the first of several large scale programs for the 6800 microprocessor. The new TSC Text Editing System is the most extensive text editor available to the micro user. It supports many of the standard commands, such as: PRINT, INSERT, DELETE, FIND, REPLACE, and VERIFY. Convenient pointer movers are provided for file TOP and BOTTOM, an APPEND command allowing any string to be appended to any or all lines starting in a specified column, text block COPY and MOVE are easily performed with a single command, and a very extensive CHANGE command allowing one to change any or all specified occurrence of one string into a second string.

Other features include, tab character definition, TAB column set, special character SET command, line NUMBERS on or off, and EXPAND tab character commands, easy pointer positioning using the NEXT command, a RENUMBER command, auto line numbering, STOP and LOG command, as well as a unique OVERLAY command, allowing the user to conveniently change a line by typing over an existing line.

A HEADER command outputs a header of column numbers also showing tab stops. A special ZONE feature allowing column restriction of all string searches and replacements is included. Special cursor control characters can be issued using the X command. Complete input control with backspace and line delete control characters are also provided. For reading and writing edited files from and to tape, READ, WRITE, and SAVE commands are provided with adjustable delays for various types of tape systems.

The editor is intended for those with serious needs. As with all TSC software, a complete source listing, hex dump listing, sample output, and complete users manual are all provided. The price for all this is only $23.50 and delivery is from stock. Order number SL68-24.

For further information contact Technical Systems Consultants, P.O. Box 2574, W. Lafayette, Indiana 47906.

CIRCLE INQUIRY NO. 132

MIKADOS

Mini Instant Keyboard Assembler, Debug, and Operating System (MIKADOS) is an assembler for developing small to moderate size programs on 6800 based microcomputer systems.

MIKADOS is specifically designed to minimize the amount of time and effort required to assemble, debug, and modify programs using a minimal amount of memory. It occupies only 2.5K bytes of memory. With only 4K bytes, this leaves 1.5K bytes which can be allocated for user programs and label table.

The assembler generates object code for the 72 basic variable-length instructions of the 6800 with all addressing mode variations. The assembler instantly generates object code for user entered mnemonics. Formatted object code and address are printed on the same line as user input. . .providing an immediate program listing. The object code is also loaded directly into user program memory. Relative branching instructions with symbolic labels are resolved by maintaining a label table for label prefixes and unresolved label operands.

There are eighteen useful directives which are 'on-line' at all times. These directives provide the user with the capability to: Input/output ASCII characters; Input hex characters, output formatted hex characters; Output formatted object code; Output formatted label table; Move data from one area of user memory to another; Clear all or any portion of user memory; Define user memory space; Start execution of user program; Set/clear breakpoints; Set/clear monitor points, plus more.

The cost is $12.95. Price includes user manual and hex object code listing.

For further information, contact INPRO Micro Systems, P.O. Box 7776, Van Nuys, CA 91409. CIRCLE INQUIRY NO. 133

Instant Input Assembler™ for TEC-9900-SS

Tired of writing programs in hex? Then our new Instant Input Assembler (IIA) is just what you have been waiting for, and it's only $49.

The Instant Input Assembler offers most standard assembler features, except labels. The unique difference is that it accepts input from the operator terminal and immediately translates it to machine code. No need to edit and punch the tape first. The assembler is delivered in two fused link PROMS (2-74S472), ready to be plugged into the existing PROM area of the Super Starter System. In addition, you will receive complete user documentation and a source listing of the amazing 512 word Instant Input Assembler. To activate the assembler, just jump to the start of it.

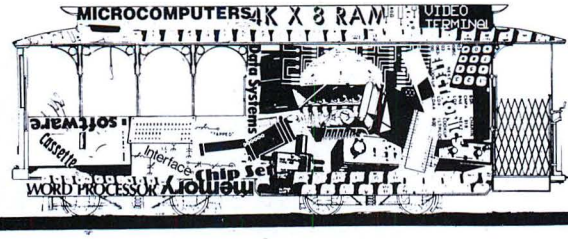
Since the IIA converts to machine language one instruction at a time, you get to see the conversion take place and printed immediately. Syntax, out of range addressing, number conversion errors are immediately rejected, so that the programmer can correct his mistakes immediately, rather than waiting for a full assembly listing.

Patching Device: existing programs under test can be immediately altered one instruction at a time without the need to re-assemble the entire program.

For further information contact Technico, 9130 Red Branch Rd., Columbia, MD. 21045. Phone 301—596-4100.

CIRCLE INQUIRY NO. 134

Watch for the "FLOPPY ROM"™ in the May issue



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- Speech Synthesis Using Home Computers
- Computers & Amateur Radio
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- Personal Computers for the Physically Handicapped
- Computers & Systems for Small Businesses
- Tutorials for Hardware Novices & Software Novices
- Software Design for Personal Computers
- Microprogrammable Microprocessors for Hobbyists
- Optical Scanning for Inexpensive Program & Data Input
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- Personal Computers in Education (associated with a University of California short-course)

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John Whitney, Pioneer Computer Film Maker under grants from Natl Endow. for Arts, Guggenheim, IBM
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LITERATURE

Books for Computerists

Dilithium Press has been formed by Merl Miller and Richard Abel. They will be publishing books on home and microcomputers for both hobbyists and people who are familiar with maxi's who want to break into micro's.

Merl Miller, the editor for the firm, is widely known for publishing books in the computer field—first at Prentice-Hall, then at West, Matrix and now at dilithium Press. Richard Abel has experience in marketing and distribution of all kinds of technical books and has also published a number of books.

The first two books to come out are by the well-known writer on computers, Richard Didday. *Home Computers:* 2^{10} QUESTIONS AND ANSWERS ABOUT HARDWARE and the companion volume *Home Computers:* 2^{10} QUESTIONS AND ANSWERS ABOUT SOFTWARE, both aimed at the beginner in the field, will tell the new micro owner what he can do—control, communications, computation, etc. They also give him the basic orientation he needs—how to read the literature, how to put a kit together and where to go from here.

The third book, *Home Computer Digital Electronics* by Merl Miller and David Irwin (chairman of the Department of Electrical Engineering and Computer Sciences at Auburn University), offers a practical introduction to the subject for the beginner. It assumes no math background, and covers logic, memories and most semi-conductor devices—so that, for instance, a person could take apart a game and make a microcomputer out of it.

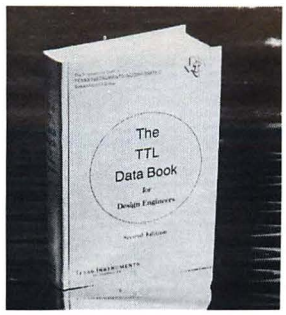
The Home Computer Primer And Glossary, by C. J. Sippl and Merl Miller, provides the fundamental knowledge and skills for the new micro owner. Part I tells him "How It Works;" Part II gives him a complete "Glossary" so that he can go on to read more advanced books with ease.

Your Introduction to Home Computers, By James Melsa and David Cohn, takes the beginner beyond the basics and shows him how to put together all he has learned and to apply it in new and exciting ways to his micro. It includes new and more advanced games; more complex and sophisticated applications; and more challenging languages and concepts.

All five of these fine books will be available this Spring. Please direct inquiries to dilithium Press, P.O. Box 92, Forest Grove, 97116.

New Edition of TTL Data Book

A new edition of a data book for design engineers on transistor-transistor logic (TTL) integrated circuits has been published by Texas Instruments Inc.



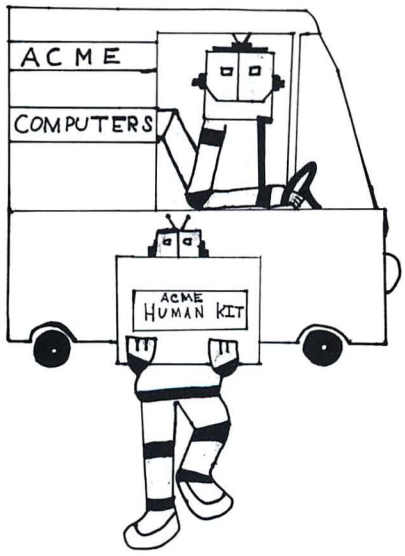
Besides combining the contents of an earlier edition and a 1974 supplement, the revised book has data on 124 new circuits. It sells for $4.95 and provides engineers and technicians with the most complete, up-to-date information available.

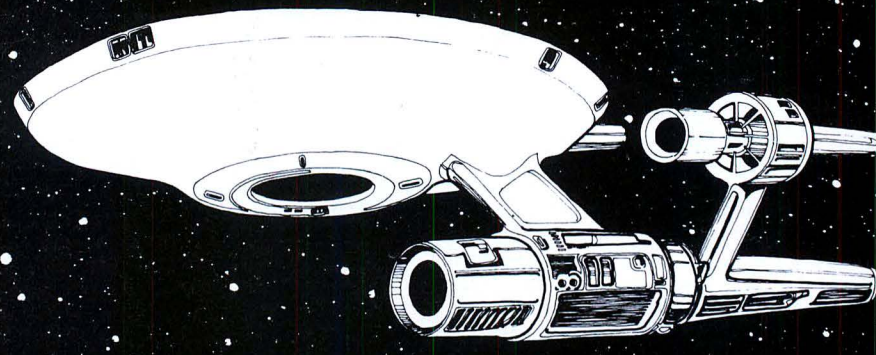
The book contains detailed specifications on over 900 Texas Instruments device types, including standard TTL and high-technology Schottky-clamped TTL. It also has pin assignment drawings of all TTL types, including bipolar memories and microprocessors.

Data on JAN integrated circuits includes cross-reference tables and a glossary section of the book has current EIA and IEC approved terms and symbols. The complete line of TI's IC sockets and interconnection panels is also covered.

Other reference aids from TI include data books on optoeletrionics, linear control circuits, semiconductor memories, transistors and diodes and power semiconductors.

For further information contact Texas Instruments Inc. Inquiry Answering Service P.O. Box 5012, M/S 84 (Attn: TTL Data Book) Dallas, Tex. 75222.





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Book Review

BASIC ELECTRICITY AND D.C. CIRCUITS (LCW8161)

by Ralph A. Oliva and Charles W. Dale with contributions by David Clemens, Ross Wise and Donald W. Taylor. Texas Instruments Incorporated. $19.95 1026 pages

Review by Judy Scolney Robertson & Larry Robertson

Basic Electricity and D.C. Circuits is an introductory electronics text designed for use in conjunction with a series of videotapes. We read the book without access to the videotapes and found it an excellent course by itself. *Basic Electricity* is oriented toward the person interested in obtaining a fundamental understanding of electronics — both digital and otherwise. The reader with some knowledge will find certain areas redundant and can easily skim over them. This repetition, however, will be most helpful to the novice using this book as a self-study course.

The book is *big!* Its size is so obvious that it is even mentioned in the "Important Note to the Student and Instructor": "This is a large-looking book of over 1000 pages . . . " About half the book is devoted to sample problems that have been worked through in detail. A significant portion of the book has also been dedicated to problem sets and examination questions to be solved by the reader who takes the course seriously.

One of a series of twenty-one solid-state electronics technology texts from the Texas Instruments Learning Center, *Basic Electricity* covers several phases of electronics, starting with a detailed discussion of how to read resistors and progressing through some rather advanced circuit analysis. The book begins with a discussion of electricity defined in terms of atomic theory. It then goes on to discuss Ohm's law, series and parallel circuits, voltage dividers and power, capacitors and the RC time constant, inductors and the LR time constant. An introduction to advanced DC circuit analysis including Kirchhoff's laws follows this basic material. A brief introduction to such advanced concepts as Thevenin's theorem, Norton's theorem and Millman's theorem is also included in the book.

Basic Electricity is concerned with only DC circuits, and thus requires only a knowledge of high school algebra for full understanding of any mathematical computations discussed. An interested person with no previous exposure to electronics would have little difficulty in clearly understanding and being able to apply the principles discussed in this text after solving all the problems presented in the problem sets. There are many examples solved and discussed in detail throughout the text. The diagrams are clear and well drawn. Mathematical relationships are presented in such a way as to facilitate their memorization and understanding.

The authors have included an outstanding glossary and a series of appendices covering everything from the Greek alphabet through a listing of the resistances of specific materials. Lists of symbols, terms, values and formulas are included for handy reference. In addition, such interesting digressions as the series of diagrams illustrating the electrical system of an automobile are included throughout the text.

Basic Electricity does not cover active components such as tubes and transistors. It is a carefully written and well tested basic first course in electronics. It is an outstanding first reference, totally suitable for self-study or classroom applications, whether used with the videotape series or by itself. Teachers and students alike will find this book to contain a clear concise well-defined presentation of the necessary materials required for an understanding of basic electronics.

Basic Electricity and D.C. Circuits is available from the Texas Instruments Incorporated Learning Center, P.O. Box 5012, Mail Station 54, Dallas, Texas 75222. Additional materials pertaining to this course are also available from the Learning Center, and include the videotape series and a laboratory manual.

A MICROPROCESSOR COURSE
FOR ENGINEERS AND PROGRAMMERS

FROM OSBORNE & ASSOCIATES, INC.
AUTHORS OF THE "INTRODUCTION TO MICROCOMPUTERS" SERIES OF BOOKS

This course teaches students how to design products around microprocessors.

This is the principal difference between a microcomputer and a minicomputer: a minicomputer is used as a vehicle for the execution of various programs; a microcomputer is used as a low cost substitute for combinatorial logic.

A microcomputer can be used, like a minicomputer, simply to execute programs; that is how microcomputers are used by computer hobbyists. Now the microcomputer user is only interested in the programming languages, and the microcomputer is packaged as a minicomputer-like system.

In sharp contrast, a logic designer who is using a microcomputer to replace combinatorial logic must look upon programming and digital logic as two interdependent aspects of microprocessor utilization.

Most microprocessor courses being taught at the present time do not accurately stress the interdependence of hardware and software. The student can go through an assembly language programming course, and the fact that a microcomputer assembly language has been taught leaves the student no closer to understanding how the microprocessor should be used. Unless assembly language is taught as an alternative to implementing transfer functions which could otherwise be implemented using combinatorial logic, students will not understand how to use microprocessors in a digital logic environment. The purpose of the course being taught by Osborne & Associates is to provide this direct comparison between hardware and programming. Students attending our course are taught how to decide whether hardware or instructions within a microcomputer system should be used in order to implement each step of any product. Emphasis is placed on giving the student a flexible understanding of whether to keep logic inside or outside the microcomputer system, how to configure the microcomputer system, and how to write programs that drive the configured microcomputer system.

Heavy emphasis is placed on classroom assignments; students are required to implement the same function using digital packages, instruction sequences within a microcomputer system, and combinations of the two.

TIME	DAY 1	DAY 2	DAY 3	DAY 4	DAY 5
8:30 - 10:00 a.m.	SESSION 1 Single Signal Logic	SESSION 4 The Central Processing Unit	SESSION 7 Assembly Language Programming	SESSION 9 Subroutines and Interrupts	SESSION 11 Parallel Interfaces
			BREAK		
10:30 a.m. - 12:00	SESSION 2 Parallel Data Concepts	SESSION 5 Memory Organization	SESSION 8 Memory Addressing Modes	SESSION 10 The 8080A CPU	SESSION 12 Serial I/O
			LUNCH		
1:00 - 2:30 p.m.	SESSION 3 The Structure Of A Microcomputer	SESSION 6 Elementary Assembly Language Programming	HANDOUT 4	HANDOUT 4 (Cont'd) HANDOUT 5	HANDOUT 5 (Cont'd)
			BREAK		
3:00 - 4:30 p.m.	HANDOUT 1/HANDOUT 2	HANDOUT 3	HANDOUT 4 (Cont'd)	HANDOUT 5 (Cont'd)	HANDOUT 5 (Cont'd)
			EVENING		
	HANDOUT 1/HANDOUT 2 (Cont'd)	HANDOUT 3 (Cont'd)	HANDOUT 4 (Cont'd)	HANDOUT 5 (Cont'd)	HANDOUT 5 (Cont'd) HANDOUT 6

TIME	DAY 6	DAY 7	DAY 8	DAY 9	DAY 10
8:30 - 10:00 a.m.	SESSION 13 Memory Systems Configurations	SESSION 15 Programming Aspects Of Interrupts	SESSION 17 The Theory Of Direct Memory Access	COMPLETE HANDOUTS	An Overview of Microcomputer Systems
			BREAK		
10:30 - 12:00	SESSION 14 One-Shots & Interval Timing; The 8253 Programmable Timer	SESSION 16 Interrupt Handling Devices	SESSION 18 The 8257 Direct Memory Access Controller	COMPLETE HANDOUTS	An Overview Of Microcomputer Systems (Cont'd)
			LUNCH		
1:00 - 2:30 p.m.	HANDOUT 6 (Cont'd) HANDOUTS 7, 8 & 9	SESSION 16 (Cont'd)	COMPLETE HANDOUTS	COMPLETE HANDOUTS	An Overview Of Microcomputer Systems (Cont'd)
			BREAK		
3:00 - 4:30 p.m.	COMPLETE HANDOUTS	COMPLETE HANDOUTS	COMPLETE HANDOUTS	COMPLETE HANDOUTS	An Overview Of Microcomputer Systems (Cont'd)
			EVENING		
	COMPLETE HANDOUTS	COMPLETE HANDOUTS	COMPLETE HANDOUTS	COMPLETE HANDOUTS	

Course fee: $600 per student at our facilities
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CIRCLE INQUIRY NO. 76

By Robert A. Stevens
Software Editor

Software Section

SUMMARY OF PROGRAMS FOR APRIL

This month's issue of INTERFACE AGE includes 2 software articles, featuring software development programs, and one game program. These programs include the following:

- Shooting Stars by Herman de Monstoy, another "universal favorite" for space buffs. Programmed in TINY BASIC 6800, the game takes only 2K of memory.
- A 6800 MIKBUG™ Extended Monitor System called EXMON by Michael Burton. EXMON extends Motorola's MIKBUG™ Monitor formware with additional needed commands. Two MIKBUG™ commands have been upgraded and ten new commands added.
- A Proposed Cassette Data Storage Format Standard and supporting 8080 Microcomputer Cassette Operating System (COS) software mechanization by Lorin Mohler provides one solution to recording cassette tapes. COS commands include Data Save, Data Load, Data Verify, and EOT commands. Data Save, Load, and Verify commands all operate on an eight ASCII character file name basis.

In addition to this month's programs I have compiled a list of 8080, 8008 and 6800 microcomputer programs available from Intel's and Motorola's user group libraries.

SOFTWARE BUGS

Dear Editor:

In your December issue you published an article on exhaustive memory testing. I ran that program for hours and did not detect any errors. In fact, however, I had one bit that would not turn off and another that would not turn on.

To find the error I used a trivial version of your published program. My version just writes every possible combination (256) of bits into every memory location and check that it could be read back correctly.

Enclosed is a copy of my version.

Gary O. Young
San Francisco

```
LOC  CONTENT                    MUI   B, O
00   0600
02   212700          LOOPI      LXI   H, START
05   78              FILL       MOV   A, B
06   77                         MOV   M, A
07   7E                         MOV   A, M
08   B8                         CMP   B
09   C21700                     JNZ   ERROR
0C   23                         INX   H
0D   7C                         MOV   A, H
DE   FE60                       CPI   60H      24K MEMORY
10   C20500                     JNZ   FILL
13   04                         INR   B
14   C30200                     JMP   LOOPI
17   00              ERROR      NOP
18   222300                     SHLD  BYTE
1B   322500                     STA   REGA
1E   78                         MOV    A, B
1F   322600                     STA   REGB
22   76                         HLT
23                   BYTE       DS    2
25                   REGA       DS    1
26                   REGB       DS    1
27                   START      EQU   1
```

HALF SIZE PROGRAM LISTINGS VS FEWER PROGRAMS UPDATE

Full size or near full size xerox copies of software published in half size format will be available from the Microcomputer Software Depository (MSD). See MSD program listing for details.

BEST ARTICLE OF THE MONTH AWARD UP-DATE

INTERFACE AGE will bestow an Honorary Award of $100.00 to the author of the best non-commercial microcomputer article of the month. Only individuals are eligible for this monthly honorarium. This monthly award is in addition to the honorarium given on the page count basis. Microcomputer articles may be on hardware, software or a combination hardware-software and will be judged by the INTERFACE AGE readership.

INTERFACE AGE SOFTWARE SHOPPING LIST

Now that INTERFACE AGE has expanded the Microcomputer software coverage and developed a large appetite for good software, your programs and application software is badly needed to quench this enlarged software appetite. This software shopping list includes the following:

- Microcomputer Development Software
- Short Software Routines
- Small Business Programs
- Hardware Control Programs
- Personal Bookkeeping Programs
- Personal Investment Programs

- Stock Market Programs
- Small Fry Educational Programs
- Software Communications Protocol Programs
- Off-Line Software Mass Storage Format Control Programs
- Game Programs
- Math Plotting Programs
- Statistics Programs
- Engineering Programs
- You Name It Programs

INEXPENSIVE MICROCOMPUTER SOFTWARE

The Microcomputer Software Depository (MSD) will act as repository for source and object code tapes. Programmers wishing to contribute programs to the public domain but who do not want to bother with distribution, may do so by forwarding appropriate documentation including short descriptive write-up and punch paper tape copy of program if possible or cassette copy to MSD. There is no membership fee for access to the public domain paper tapes (PDT) from MSD.

Anyone may obtain copies of these PDT software packages by prepaying a small fee with the order to cover duplication, postage and handling cost. Prices will be listed periodically in INTERFACE AGE. Typical cost for a short program will be approximately $5.00 ($3.00/ounce) + tax, postage and handling. As a convenience MSD will also provide punched paper tape copies of vendor supplied software packages (VSP) that will be sold at vendor suggested sale prices. For a current copy of the available software from the Microcomputer Software Depository (MSD) send a check for $1.00 with a prestamped 9″ x 12″ return envelope to MSD.

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MICROCOMPUTER SOFTWARE DEPOSITORY PROGRAM LISTING

THE FOLLOWING LISTS SOFTWARE AVAILABLE FROM MSD ON A PREPAID BASIS
ONLY. THE TOTAL COST OF EACH PACKAGE IS THE SUM OF THE BASIC PRICE
+ CALIFORNIA SALES TAX, IF APPLICABLE, + POSTAGE AND HANDLING COST.
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MICROCOMPUTER SOFTWARE DEPOSITORY (MSD) PROGRAMS  DATE APRIL 1977 REV.0

PROGRAM MEDIA                          NOTES
PTAC  PAPER TAPE ASSEMBLY CODE         *  CALIF. SALES TAX REQUIRED
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PTSC  PAPER TAPE SOURCE CODE                    FROM RESIDENCE OF CALIF.
PTOC  PAPER TAPE OBJECT CODE                :   USA POSTAGE + HANDLING OR
PTBC  PAPER TAPE BASIC CODE                     THIRD CLASS USA POSTAGE +
PTAL  PAPER TAPE ASSEMBLY LISTING               HANDLING OR SURFACE RATE
PTSL  PAPER TAPE SOURCE LISTING                 FOREIGN POSTAGE  @
PTOL  PAPER TAPE OBJECT LISTING                 THREE TIMES THIRD CLASS
PTOD  PAPER TAPE OBJECT DUMP                    USA POSTAGE RATE(STANDARD
PTBL  PAPER TAPE BASIC LISTING                  OR SURFACE RATE FOREIGN
CTAL  CASSETTE TAPE ASSEMBLY LISTING            POSTAGE @ FIVE TIMES USA
CTSL  CASSETTE TAPE SOURCE LISTING              POSTAGE RATE (ALTERNATE)
CTOL  CASSETTE TAPE OBJECT LISTING          >   NEW PROGRAM LISTING
CTOD  CASSETTE TAPE OBJECT DUMP             %   VENDOR SOFTWARE PACKAGE -
CTBC  CASSETTE TAPE BASIC CODE
CTBL  CASSETTE TAPE BASIC LISTING
HCAC  XEROX HARD COPY OF ASSEMBLY CODE
HCSC  XEROX HARD COPY OF SOURCE CODE
HCOC  XEROX HARD COPY OF OBJECT CODE
HCBC  XEROX HARD COPY OF BASIC CODE
HCAL  XEROX HARD COPY OF ASSEMBLY LISTING
HCALF FULL SIZE XEROX HARD COPY OF ASSEMBLY LISTING
HCSL  XEROX HARD COPY OF SOURCE LISTING
HCOL  XEROX HARD COPY OF OBJECT LISTING
HCOD  XEROX HARD COPY OF OBJECT DUMP
HCBL  XEROX HARD COPY OF BASIC LISTING
TEXT  XEROX HARD COPY OF PRINTED TEXT
PTTL  PAPER TAPE TEXT LISTING
CTTL  CASSETTE TAPE TEXT LISTING
MAN   MANUAL
HCGR  XEROX HARD COPY OF GRAMMAR
PTGR  PAPER TAPE COPY OF GRAMMAR
RBSL  XEROX HARD COPY OF BINARY BOOTSTRAP LOADER
HBSL  XEROX HARD COPY OF HEX BOOTSTRAP LOADER
PACK  PACKAGE PRICE INCLUDES ALL ITEMS/PROGRAM # WITH SYMBOL <

      SUFFIX C= HAND ASSEMBLED CODE
      SUFFIX L= COMPUTER FORMATED LISTING
      SUFFIX D= CODE DUMP IN OCTAL OR HEX
      SUFFIX F= FULL SIZE COPY

DEFINITIONS:

  ASSEMBLY LISTING: COMPUTER ASSEMBLED SOFTWARE PROGRAM LISTING
                    THAT INCLUDES SYMBOLIC ASSEMBLY LANGUAGE SOURCE
                    CODED INSTRUCTIONS WITH COMMENTS PLUS
                    EQUIVALENT MACHINE LANGUAGE OBJECT CODED
                    INSTRUCTINS AND MEMORY ADDRESS ASSIGNMENTS FOR
                    EACH INSTRUCTION ( SOURCE + OBJECT ).

  ASSEMBLY CODE:    SAME CONTENT AS ASSEMBLY LISTING BUT HAND ASSEMBLED.

  SOURCE LISTING:   SOFTWARE PROGRAM LISTING RESULTING FROM COMPUTER
                    SOFTWARE CONTROLLED ASSEMBLY PROCESS THAT INCLUDES
                    ASSEMBLY LANGUAGE SOURCE CODED INSTRUCTIONS WITH
                    COMMENTS. SOMETIMES, LINE STATEMENT NUMBERS ARE
                    INCLUDED FOR EACH INSTRUCTION.

  SOURCE CODE:      SAME CONTENT AS SOURCE LISTING BUT HAND ASSEMBLED.

  OBJECT LISTING:   SOFTWARE PROGRAM LISTING RESULTING FROM COMPUTER
                    SOFTWARE CONTROLLED ASSEMBLY PROCESS THAT ONLY
                    INCLUDES MACHINE READABLE OBJECT CODED INSTRUCTIONS
                    AND MEMORY ADDRESS ASSIGNMENTS.

  OBJECT CODE       SAME CONTENT AS OBJECT LISTING BUT HAND ASSEMBLED.

  HARD COPY:        XEROX OR PRINTED COPY.

  CODE:             HAND ASSEMBLED CODE ( SOURCE, OBJECT, OR ASSEMBLY
                    CODE ).

  LISTING:          COMPUTER FORMATED LISTING.

  DUMP:             COMPUTER MEMORY DUMP.
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MSD PROGRAMS

CPU TYPE	SYMBOLIC NAME	DESCRIPTIVE NAME	MSD # & MEDIA	P A C K	R E V #	+CALIF. TAX(*) +USA POSTAGE(:)
6502	APPLECD	6502 APPLE COMPUTER DISASSEMBLER BY ALLEN BAUM & STEPHEN WOZNIAK-INTERFACE AGE, SEPT. 1976, VOL.1,#10.	1-TEXT 1-HCAL 1-PACK	< < ↑		5.00+0.30+1.00 INC. WITH TEXT
8080	LPTIIHF	LOAD 8080 PAPER TAPE IN INTEL HEX FORMAT BY BURT HASHIZUME-INTERFACE AGE, OCT. 1976, VOL.1,#11.	2-PTAL 2-TEXT 2-HCAL 2-PACK	< Ø < < ↑		8.00+0.48+2.00 3.00+0.18+1.00 INC. WITH TEXT
8080	BFWOA	8080 BINARY FILES WITH OPTIONAL AUTOSTART BY WILLIAM H. JORDAN-INTERFACE AGE, OCT. 1976, VOL.1,#11.	3-PTAL 3-PTOD 3-TEXT 3-HCAL 3-PACK	< Ø < < < ↑		8.00+0.48+1.00 INC. WITH PTAL 3.00+0.18+1.00 INC. WITH TEXT
6800	MINOPS	MIN OPERATING SYSTEM BY ED KEITH & DENNIS HESCOX-INTERFACE AGE, OCT. 1976, VOL.1,#11. PTAL+ INCLUDES OPERATING INSTRUCTIONS, PAPER TAPE FORMAT AND SAMPLE RUN	4-PTAL+ 4-PTOD 4-TEXT 4-HCAL 4-PACK	< Ø < < < ↑		8.00+0.48+2.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH TEXT
8080	DBBDP	DR. BEATTIE'S BASIC DIET PLANNING BY DR. BEATTIE-INTERFACE AGE, OCT. 1976, VOL.1,#11.	5-TEXT 5-HCBL 5-PTBL 5-PACK	< Ø < < ↑		3.00+0.18+1.00 INC. WITH TEXT 8.00+0.48+2.00
6800	EZMERPS	ECHO 1, ZERO MEMORY, ECHO REVERSE & PRINT SUBROUTINES BY HOWARD BERENSON-INTERFACE AGE, OCT. 1976, VOL.1,#11.	6-PTAL 6-TEXT 6-HCAL 6-PACK	< Ø < < ↑		5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH TEXT
8080	ESP-1	ESP-1 SOFTWARE PACKAGE BY MICHAEL SHRAYER-INTERFACE AGE, OCT. 1976, VOL.1,#11.	7-PTOD 7-MAN 7-CTOD	<%Ø < <		30.00+1.80+1.50 INC. WITH PTOD 30.00+1.80+1.50
		PTGR IS PAPER TAPE COPY OF GRAMMAR.	7-MAN 7-PTGR 7-HCGR 7-PACK	< < < ↑		INC. WITH CTOD 5.00+0.30+1.50 INC. WITH PTGR
8080	PTSP-1	PROCESSOR TECHNOLOGY SOFTWARE PACKAGE NO. 1 SUMMARY BY R. A. STEVENS-INTERFACE AGE, OCT. 1976, VOL.1,#11.	8-PTGR 8-TEXT 8-PACK	<%Ø < ↑		5.00+0.30+1.50 INC. WITH PTTL
8080	EXAMMT	EXHAUSTIVE 8080 RAM MEMORY TEST PROGRAM BY T.F.TRAVIS-INTERFACE AGE, NOV. 1976, VOL.1,#12.	9-PTAL 9-PTOD 9-TEXT 9-HCAL 9-HCOD 9-PACK	< Ø < < < < ↑		6.00+0.36+2.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH TEXT INC. WITH TEXT
6800	MEMDMP-1	SWTPC 6800 MEMORY DUMP PROGRAM MEMDMP-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1,#12.	10-PTAL 10-PTSL 10-PTOD 10-TEXT 10-HCAL 10-PACK	< Ø < Ø < < < ↑		5.00+0.30+1.00 8.00+0.48+1.00 INC. WITH PTSL 1.00+0.06+1.00 INC. WITH TEXT
6800	ROBIT-1	SWTPC 6800 ROTATING BIT RAM MEMORY DIAGNOSTIC PROGRAM ROBIT-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1,#12.	11-PTAL 11-PTSL 11-PTOD 11-TEXT 11-HCAL 11-PACK	< Ø < Ø < < < ↑		5.00+0.30+1.00 8.00+0.48+1.00 INC. WITH PTSL 1.00+0.06+1.00 INC. WITH TEXT
6800	MEMCON-1	SWTPC 6800 SHORT MEMORY ADDRESS CONVERGENCE PROGRAM MEMCON-1 BY GARY KAY-INTERFACE AGE, NOV. 1976, VOL.1,#12.	12-PTAL 12-PTSL 12-PTOD 12-TEXT 12-HCAL 12-PACK	< Ø < Ø < < < ↑		5.00+0.30+1.00 8.00+0.48+1.00 INC. WITH PTSL 1.00+0.06+1.00 INC. WITH TEXT
6800	BJIB	BLACKJACK IN BASIC PROGRAM BY ED KEITH & DENNIS HESCOX. THE BJIB PAPER TAPE OBJECT CODE REQUIRES ROBERT UITERWYK'S SWTPC MICROBASIC OPERATING SYSTEM-INTERFACE AGE, NOV. 1976, VOL.1,#12. PTBL+ INCLUDES SAMPLE RUN, INSTRUCTIONS, LIST OF VARIABLES AND LIST OF ROUTINES.	13-PTBL 13-PTBL+ 13-TEXT 13-HCBL 13-PACK	Ø < < < ↑		9.00+0.54+2.00 12.00+0.72+2.00 2.00+0.12+1.00 INC. WITH TEXT

6502	RFPR	REVISED FLOATING POINT ROUTINES FOR 6502* BY ROY RANKIN & STEVE WOZNIAK - INTERFACE AGE, NOV. 1976, VOL.1,#12. NOTE * - ORIGINAL MATH PACKAGE FIRST APPEARED IN DR. DOBB'S JOURNAL, AUG. 1976, VOL.1,#7.	14-PTOD < 1 14-PTAL < 14-PTSL < 14-TEXT < 14-HCAL < 14-PACK ↑	5.00+0.30+1.00 9.00+0.54+2.00 10.00+0.60+2.00 2.00+0.12+1.00 INC. WITH TEXT
6800	HISPDMUP	HIGH SPEED DOUBLE PRECISON MULTIPLICATION SUBROUTINE- HISPDMUP BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY- INTERFACE AGE, NOV. 1976, VOL.1,#12.	15-PTAL < 0 15-TEXT < 15-HCAL < 15-PACK ↑	8.00+0.48+1.00 1.00+0.06+1.00 INC. WITH TEXT
6800	DIV16	REENTRANT 16 BIT DIVIDE SUBROUTINE - DIV16 BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY- INTERFACE AGE, NOV. 1976, VOL.1,#12.	16-PTAL < 1 16-TEXT < 16-HCAL < 16-PACK ↑	8.00+0.48+1.00 1.00+0.06+1.00 INC. WITH TEXT
6800	RENTMUP	REENTRANT DOUBLE PRECISION MULTIPLICATION SUBROUTINE- RENTMUP BY PERMISSION AND COURTESY OF MOTOROLA'S M6800 USER GROUP LIBRARY- INTERFACE AGE, NOV. 1976, VOL.1,#12.	17-PTAL < 0 17-TEXT < 17-HCAL < 17-PACK ↑	8.00+0.48+1.00 1.00+0.06+1.00 INC. WITH TEXT
8080	HOMEC	COMPUTER OR CONTROLLER BY TERRY BENSON, INTEL - INTERFACE AGE, SEPT. 1976, VOL.1,#10.	18-PTAL < 0 18-PTSL < 18-TEXT < 18-HCAL < 18-PACK ↑	5.00+0.30+1.00 5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH TEXT
8080	LCST	STARTREK BY LYNN COCHRAN- INTERFACE, JUNE 1976, VOL.1,#7.	19-PTBL < 0 19-TEXT < 19-HCBL < 19-PACK ↑	7.00+0.42+1.00 3.00+0.18+1.00 INC. WITH TEXT
8080	WSPG	WORD SEARCH PUZZLE GENERATOR BY RICHARD S. EDELMAN - INTERFACE, JULY 1976, VOL.1,#8.	20-PTBL < 0 20-TEXT < 20-HCBL < 20-PACK ↑	6.00+0.36+1.00 2.00+0.12+1.00 INC. WITH TEXT
8080	PGBIORHY	BIORHYTHM BY PAUL GREEN - INTERFACE AGE, AUG. 1976, VOL.1,#9.	21-PTBL < 0 21-TEXT < 21-HCBL < 21-PACK ↑	6.00+0.36+1.00 1.00+0.12+1.00 INC. WITH PTBL
8080	WDBIORHY	BIORHYTHMS IN PRACTICE BY WILLIAM L. DONHAN, M.D. - INTERFACE AGE, AUG. 1976, VOL.1,#9.	22-PTBL < 0 22-TEXT < 22-HCBL < 22-PACK ↑	8.00+0.48+2.00 2.00+0.12+1.00 INC. WITH TEXT
8080	REBJ	BLACKJACK BY RICHARD S. EDELMAN - INTERFACE AGE, AUG. 1976, VOL.1,#9.	23-PTBL < 0 23-TEXT < 23-HCBL < 23-PACK ↑	6.00+0.36+1.00 1.00+0.06+1.00 INC. WITH TEXT
8080	BLUFF	BLUFF BY PHIL FELDMAN & TOM RUGE - INTERFACE AGE, SEPT. 1976, VOL.1,#10.	24-PTBL < 0 24-TEXT < 24-HCBL < 24-PACK ↑	6.00+0.36+1.00 1.00+0.06+1.00 INC. WITH TEXT
6800	RABSIMB	RELATIVE ADDRESS BACK-STEPPER IN MICRO-BASIC BY J. HUFFMAN - INTERFACE AGE, DEC. 1976, VOL.1,#13.	25-PTBL < 0 25-HCBL < 25-TEXT < 25-PACK ↑	5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH HCBL
6800	TEFT6800	TEXT EDITOR FOR THE SWTPC-6800 BY MARK BOKGERSON - INTERFACE AGE, DEC. 1976, VOL.1,#13. HCAL IS COPY OF FULL SIZE ASSEMBLY LISTING.	26-PTAL < 0 26-PTOD < 26-HCAL < 26-TEXT < 26-PACK ↑	15.00+0.90+2.00 10.00+0.60+2.00 3.00+0.18+1.50 2.00+0.12+1.25
8080	WPATRX	WANG'S PALO ALTO TINY BASIC BY ROGER RAUSKOLB - INTERFACE AGE, DEC. 1976, VOL.1,#13. HCAL & HCSL ARE COPIES OF FULL SIZE CODE	27-PTSL < 0 27-PTOD < 27-HCAL < 27-TEXT < 27-HCSL < 27-PACK ↑	20.00+1.20+3.00 10.00+0.60+2.00 4.00+0.24+1.50 INC. WITH HCAL 4.00+0.24+1.50
8080	LLLBI	LLL 8080 BASIC INTERPRETER GRAMMAR BY JERRY BARBER & ROYCE ECKARD - SUBMITTED BY E.R. FISHER - INTERFACE AGE, DEC. 1976,VOL.2,#1(PART 1). JAN. 1977,VOL.2,#2(PART 2), FEB. 1977,VOL.2,#3(PART 3), MARCH 1977,VOL.2,#4(PART 4). TEXT1 IS PART 1,' TEXT2 IS PART 2, ETC. HCAL2,3, & 4 ARE FULL SIZE XEROX COPIES OF ASSEMBLY PROGRAM LISTINGS OF PARTS 2,3, & 4.	28-TEXT1< 0 28-HCAL2< 28-TEXT2< 28-HCAL3< 28-TEXT3< 28-TEXT4< 28-HCAL4<	5.00+0.30+2.00 5.00+0.30+2.00 3.00+0.18+2.00 5.00+0.30+2.00 3.00+0.18+2.00 3.00+0.18+2.00 3.00+0.18+2.00
SC/MP	NIBL	NIBL-NATIONAL'S TINY BASIC GRAMMAR FOR SC/MP BY PHIL ROYBAL - INTERFACE AGE, DEC. 1976, VOL.2, #1. ASSEMBLY LISTING PUBLISHED JAN. 1977, VOL.2,#1.	29-TEXT < 0 29-HCAL < 29-PTSL < 29-PTOD < 29-PTGR < 29-PACK ↑	5.00+0.30+2.00 10.00+3.00+2.00 10.00+3.00+2.00 5.00+1.50+1.00 2.00+0.12+1.00
SC/MP	MYBAGELS	BAGELS BY DR. MARVIN WINZINKEAD BY PERMISSION & COURTESY OF NATIONAL SEMICONDUCTOR - INTERFACE AGE, DEC. 1976, VOL.2,#1.	30-PTBL < 0	5.00+0.30+2.00
8080	AMS80	AMSAT 8080 STANDARD DEBUG MONITOR BY RICHARD C ALLEN & JOE KASSER - BYTE # 13, SEPT. 1976, VOL.2,#1. SUBMITTED BY JOE KASSER.	31-PTSL < 2 31-PTOD < 31-PACK ↑	15.00+0.90+2.00 5.00+0.30+2.00
6800	BAFCMP	BASIC ALGORITHMS FOR COMMON MATH FUNCTIONS BY MICHAEL P. BURTON - INTERFACE AGE, JAN. 1977, VOL.2,#2.	32-PTBL < 1 32-TEXT < 32-PACK ↑	6.00+0.36+1.00 2.00+0.12+1.00
8080	ECMSO	MICROCOMPUTER STOCK OPTIONS BY EDWARD CHRISTIANSON - INTERFACE AGE, FEB. 1977, VOL.2,#3.	33-PTBL < 0 33-HCBLF 33-HCBLF< 33-TEXT < 33-PACK ↑	15.00+0.90+2.00 5.00+0.30+2.00 INC. WITH PTBL 5.00+0.30+2.00
8080	RMRNG	RANDOM NUMBER GENERATOR BY BOB MARTIN - INTERFACE AGE, FEB. 1977, VOL.2,#3.	34-PTAL < 0 34-PTSL < 34-TEXT < 34-HCALF 34-HCALF< 34-PACK ↑	7.00+0.42+2.00 6.00+0.36+2.00 2.00+0.12+1.00 4.00+0.24+1.00 INC. WITH PTAL
8080	RNDFGCST	RND FUNCTION GENERATOR CHI-SQUARE TEST PROGRAM BY BOB MARTIN - INTERFACE AGE, FEB. 1977, VOL.2,#3.	35-PTBL < 35-HCBLF< 35-PACK ↑	4.00+0.24+1.00 INC. WITH PTBL
8080	TTMOCSR	8080 MEMORY OBJECT CODE SEARCH ROUTINE BY T. E. TRAVIS - INTERFACE AGE, FEB. 1977, VOL.2,#3.	36-PTAL < 0 36-PTSL < 36-TEXT < 36-HCALF< 36-HCALF 36-PACK ↑	5.00+0.30+1.00 5.00+0.30+1.00 1.00+0.06+1.00 INC. WITH TEXT 2.00+0.12+1.00
8080	TDOMP	8080 OCTAL MONITOR PROGRAM BY THOMAS E. DOYLE - INTERFACE AGE, FEB. 1977, VOL.2,#3.	37-PTAL < 0 37-PTSL < 37-TEXT < 37-HCALF 37-HCALF< 37-PTOD < 37-PACK ↑	8.00+0.48+2.00 8.00+0.48+2.00 2.00+0.12+1.00 4.00+0.24+1.00 INC. WITH PTAL 5.00+0.30+1.50
8080	LLLBFPMP	LLLBASIC FLOATING POINT MATH PACKAGE BY DAVID MEAD & MODIFIED BY HAL BRAND AND FRANK OLKEN - INTERFACE AGE, FEB. 1977, VOL.2,#3.	38-TEXT < 0 38-HCALF<	3.00+0.18+2.00 5.00+0.12+2.00
8080	Z80MERP	Z80 MITS 12K EXTENDED BASIC PATCHES BY MARTIN D. GRAY - INTERFACE AGE, MARCH 1977, VOL.2,#4.	39-TEXT < 0 39-HCALF< 39-PACK ↑	1.00+0.06+1.00 1.00+0.06+1.00
6502	RJBAST	6502 APPLE STAR-TREK BY ROBERT J. BISHOP - INTERFACE AGE, APRIL 1977, VOL.2,#5.	40-TEXT < 0 40-HCBL < 40-PACK ↑	3.00+0.18+1.00 INC. WITH TEXT
6800	AMIPROTO	AMI'S PROTO DEVELOPMENT SOFTWARE FOR EVK SERIES PROTOTYPING BOARDS BY PERMISSION AND COURTESY OF AMERICAN MICROSYSTEMS EDITED BY R.A.STEVENS- INTERFACE AGE, FEB. 1977, VOL.2,#3.	41-TEXT < 0 41-HCALF< 41-PACK ↑	3.00+0.18+1.00 5.00+0.30+2.00
8080	CONSOL	CONSOL 1K RESIDENT OPERATING SYSTEM BY PERMISSION AND COURTESY OF PROCESSOR TECHNOLOGY- INTERFACE AGE, JAN. 1977, VOL.2,#2.	42-TEXT < 0 42-HCALF< 42-PACK ↑	3.00+0.18+1.00 5.00+0.30+2.00
8080	ODT-80	LLL BASIC OCTAL DEBUGGING PROGRAM BY E. R. FISHER- INTERFACE AGE, MARCH 1977, VOL.2,#4.	43-TEXT < 0 43-HCALF< 43-PACK ↑	3.00+0.18+2.00 5.00+0.30+2.00
6800	(RS)*3	RESIDENT 6800 REENTRANT SELF-RELATIVE SUBROUTINE PACKAGE FOR EVK 6800 MICROCOMPUTER BOARDS BY PERMISSION AND COURTESY OF AMERICAN MICROSYSTEMS EDITED BY R.A. STEVENS- INTERFACE AGE, MARCH 1977, VOL.2,#4.	44-TEXT < 0 44-HCALF< 44-PACK ↑	3.00+0.18+1.00 5.00+0.30+2.00
6800	EXMON	6800 MIKBUG EXTENDED MONITOR SYSTEM BY MICHAEL BURTON- INTERFACE AGE, APRIL 1977, VOL.2,#5.	45-TEXT < 0 45-HCALF< 45-PTAL < 45-PTOD < 45-PACK ↑	2.00+0.12+1.00 3.00+0.18+1.50 9.00+0.54+2.00 5.00+0.30+2.00
8080	LMCOS	8080 CASSETTE OPERATING SYSTEM (COS) BY LORIN MOHLER- INTERFACE AGE, APRIL 1977, VOL.2,#5.	46-TEXT < 46-PTSL < 46-HCALF< 46-PACK ↑	3.00+0.18+1.00 10.00+0.60+2.00 5.00+0.30+1.00
6800	MHFTIHFC	MOTOROLA 6800 HEX FORMAT TO INTEL FORMAT SOFTWARE CONVERTER BY FLOYD NORDIN- INTERFACE AGE, APRIL 1977, VOL.2,#5.	47-TEXT < 0 47-PTAL < 47-PTSL < 47-PTOD < 47-HCALF< 47-HCODF< 47-PACK ↑	1.00+0.06+1.00 5.00+0.30+2.00 5.00+0.30+2.00 3.00+0.18+1.00 3.00+0.18+1.00 INC. WITH HCAL
8080	MMGTEW	GRAPHICS- THE EASY WAY BY MARVIN MALLON- INTERFACE AGE, MARCH 1977, VOL.2,#4.	48-TEXT 0 48-HCBLF	3.00+0.18+1.00 5.00+0.30+1.00
8080	CBMS	BYTEMOVER SOFTWARE FOR THE CROMEMCO 8K BYTESAVER BOARD - PERMISSION AND COURTESY OF CROMEMCO EDITED BY ROGER EDELSON- INTERFACE AGE, JAN. 1977, VOL.2,#2.	49-TEXT 0 49-HCAL	5.00+0.30+1.00 INC. WITH TEXT
8080	FNOCDA	8080 OBJECT CODE DIS-ASSEMBLER BY FLOYD L. NORDIN- STANDARD VERSION HANDLES UP TO 1K LABLES & ASSIGNS SYMBOLIC NAMES. ASCII CHARACTER LIST PIN POINTS EMBEDDED TABLES. INCLUDES BOTH ASSEMBLY AND SOURCE OUTPUT MODES VIA YOUR OUTPUT DRIVERS. PROGRAM RESIDES AT TOP OF MEMORY. STANDARD VERSIONS AVAILABLE FOR 16K, 24K, 32K, 48K AND 64K BYTES OF MEMORY.	50-PTOD <%0 50-MAN < 50-PACK ↑	40.00+2.40+2.00 5.00+0.30+1.00 45.00+2.70+3.00

		OTHER VERSIONS WITH ADDITIONAL LABLE SPACE AND/OR DIFFERENT MEMORY SIZE ARE AVAILABLE.		
6800	SWTPMB	SWTP'S 6800 MICROBASIC VER. 1.4 BY ROBERT H. UITERWYK AND BY PERMISSION & COURTESY OF SOUTHWEST TECHNICAL PRODUCTS CORP. SWTPC 6800 COMPUTER NEWSLETTER #1, JUNE 1976.	51-PTOD Ø	15.00+0.90+2.00
6800	EVKMB	SWTP'S 6800 MICROBASIC VER. 1.4 MODIFIED FOR AMI'S 6800 EVK MICROCOMPUTER BOARDS BY STEVEN D. WALL.	52-PTOD Ø	15.00+0.90+2.00
8080	CCOKEN	ARTIFICAL INTELLIGENCE TIC-TAC-TOE PROGRAM (OR MENACE OF THE MICROWORLD) BY KEN BERKUM -INTERFACE AGE, MARCH 1977, VOL.2,#4.	53-PTBL < Ø 53-TEXT < 53-HCBL < 53-HCBL 53-PACK †	10.00+0.60+2.00 2.00+0.12+1.00 INC. WITH PTBL 2.00+0.12+1.00
6800	JHDOTWP	DAY OF THE WEEK PROGRAM BY JIM HUFFMAN-INTERFACE AGE, APRIL 1977, VOL.2,#5.	54-PTBL < Ø 54-TEXT < 54-HCBL < 54-HCBL 54-PACK †	6.00+0.36+1.00 1.00+0.06+1.00 INC. WITH PTBL 1.00+0.06+1.00
6800	JHCRBP	CHECKBOOK BALANCER PROGRAM BY JIM HUFFMAN - INTERFACE AGE, APRIL 1977, VOL.2,#5.	55-PTBL < Ø 55-TEXT < 55-HCBL < 55-HCBL 55-PACK †	6.00+0.36+1.00 1.00+0.06+1.00 INC. WITH PTBL 1.00+0.06+1.00
8080	HEXDUMP	INTEL HEX FORMAT PAPER TAPE DUMP PROGRAM BY ALAN R. MILLER - INTERFACE AGE, APRIL 1977, VOL.2,#5.	56-PTAL < 1 56-PTSL < 56-PTOD < 56-HCAL < 56-HCAL 56-HCSL < 56-HCSL 56-PACK †	8.00+0.48+2.00 8.00+0.48+2.00 5.00+0.30+1.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH PTSL 2.00+0.12+1.00
8080	CONVERT1	NUMBER BASE CONVERSION-NON DISC VERSION BY JOHN W. SWAIN- INTERFACE AGE, APRIL 1977, VOL.2,#5.	57-PTBL < Ø 57-TEXT < 57-HCBL < 57-HCBL 57-PACK †	7.00+0.42+1.00 2.00+0.12+1.00 INC. WITH PTBL 1.00+0.06+1.00
8080	CONVERT2	NUMBER BASE CONVERSION-DISC BASED VERSION OF CONVERT1 ABOVE BY JOHN W. SWAIN - INTERFACE AGE, APRIL 1977, VOL.2,#5.	58-PTBL < Ø 58-TEXT < 58-HCBL < 58-HCBL 58-PACK †	7.00+0.42+1.00 2.00+0.42+1.00 INC. WITH PTBL 1.00+0.06+1.00
Z80	SERIAL	USER TTY HANDLER FOR THE Z80 DELEVOPMENT SYSTEM BY RICHARD E. MALY - INTERFACE AGE, APRIL 1977, VOL.2,#5.	59-TEXT Ø 59-HCAL	3.00+0.18+1.00 2.00+0.12+1.00
6800	MEMTEST	A BETTER 6800 MEMORY TEST BY ED KEITH- INTERFACE AGE, APRIL 1977, VOL.2,#5.	60-PTAL < Ø 60-PTSL < 60-PTOD < 60-TEXT < 60-HCAL < 60-HCAL 60-HCSL < 60-HCSL 60-PACK †	8.00+0.48+2.00 8.00+0.48+2.00 3.00+0.18+1.00 2.00+0.12+1.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH PTSL 2.00+0.12+1.00
8080	AMLIFE	JOHN CONWAY'S GAME OF LIFE PROGRAMMED BY ALAN R. MILLER -INTERFACE AGE, APRIL 1977, VOL.2,#5.	61-PTAL < 4 61-PTSL < 61-PTOD < 61-TEXT < 61-HCAL < 61-HCAL 61-HCSL < 61-HCSL 61-PACK †	15.00+0.90+2.00 10.00+0.60+2.00 5.00+0.30+1.00 2.00+0.12+1.00 INC. WITH PTAL 2.00+0.12+1.00 INC. WITH PTSL 2.00+0.12+1.00
8080	SFSL	STAR LANES PROGRAM BY STEVEN FABER - INTERFACE AGE, APRIL 1977, VOL.2,#5.	62-PTBL < Ø 62-HCBL < 62-TEXT < 62-HCBL < 62-HCBL 62-PACK †	15.00+0.60+2.00 2.00+0.12+1.00 2.00+0.12+1.00 INC. WITH PTBL 2.00+0.12+1.00

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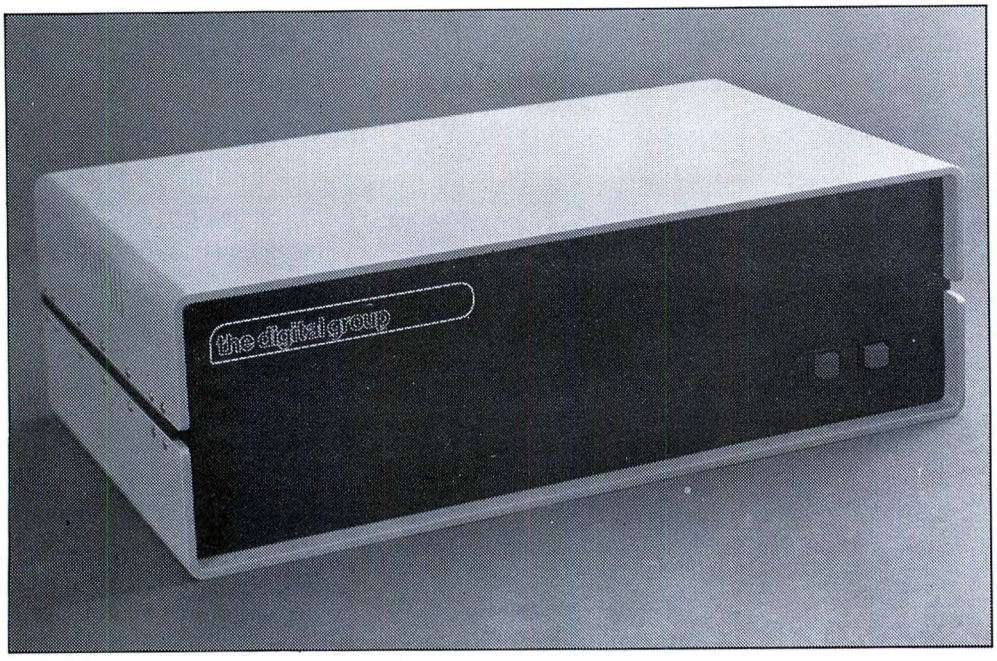

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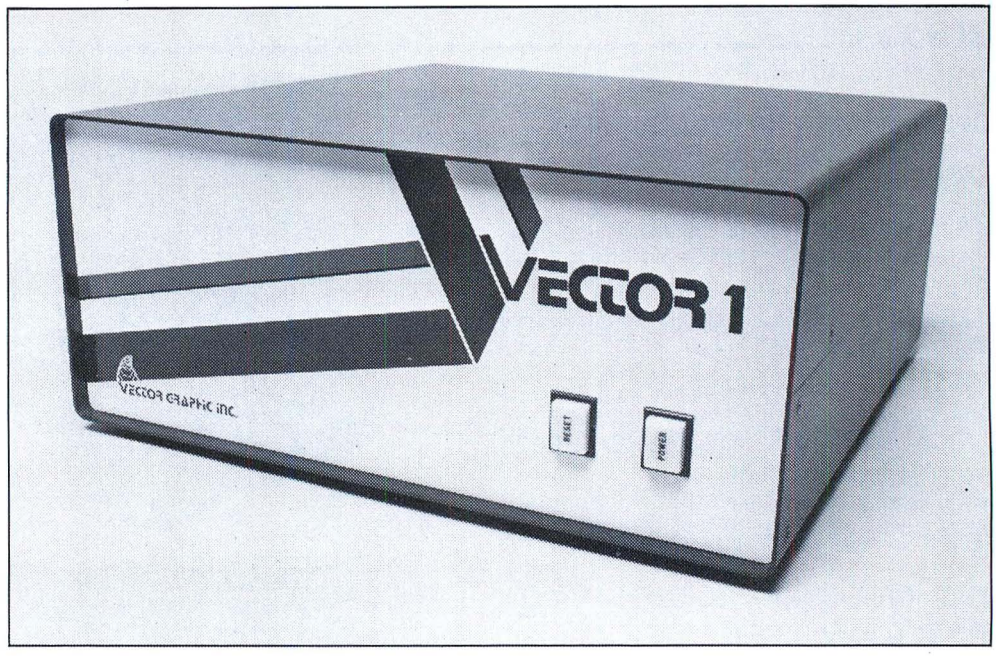

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Shooting Stars

by H. DeMonstoy

INTRODUCTION

This game was written to run on my SWTP 6800 with the CT-1024 terminal. The Basic program is Tom Pittman's "TINY BASIC 6800" from Itty Bitty Computers. Tom Pittman's Tiny BASIC takes about 2K of memory.

The idea for this game came from BYTE's May 76 issue, but I have seen it in several forms from high level language to a game for the calculator. I wrote this program to fit my needs with the Tiny Basic and TV terminal.

RULES OF THE GAME

The game is played in a "universe" of stars (★) and black holes (–) that is arranged in a 3 X 3 matrix. Each position has its own number from one to nine. Position 1, 2 and 3 are across the top, with 4, 5 and 6 through the center and 7, 8 and 9 across the bottom. The first print out has a star in the center (position 5) with black holes all around it. The idea is to shoot stars only, never a black hole, and change the "universe" into eight stars surrounding one black hole.

Each star has its own "galaxy", and when a star is hit, every position in that galaxy changes: all stars become black holes, and all black holes become stars. The first shot must be position 5, the only star in the universe. When this is done, position 5 becomes a black hole and position 2 (above), position 4 (left), position 6 (right), and position 8 (below) all become stars. So it goes on and on. The best score is eleven shots, but watch out for the all black hole "universe" because it is a loser; no stars left to shoot.

The instruction subroutine has a "galaxy" map to follow. Each one is different, which makes for an interesting challenge.

FRAME NUMBERS DISPLAYED FOR ADDED INTEREST

For added interest the frame number is printed in the first line of each frame to keep a running count of the trys. The record here is 56 trys before a win. By the way, I think the quickest loss is in 5 trys, but I may be proven wrong.

CRT TERMINAL CONTROL

As I mentioned before this program was written for the CT-1024 TV terminal and so has some special statements to control the cursor. In my system the "Home Up" is a CONTROL P (DEL), and "Erase to EOL" is a CONTROL U (NAK), but may be different in your system. These do not show in the written program, but are used 4 times. The first is line 149 where, after 3 frames, a new start is made at the top of the screen. The control signals are located in the quotation marks after the PRINT statement. Lines 900, 919, and 939 are similar, and start the three instruction frames.

TTY TERMINAL CONTROL

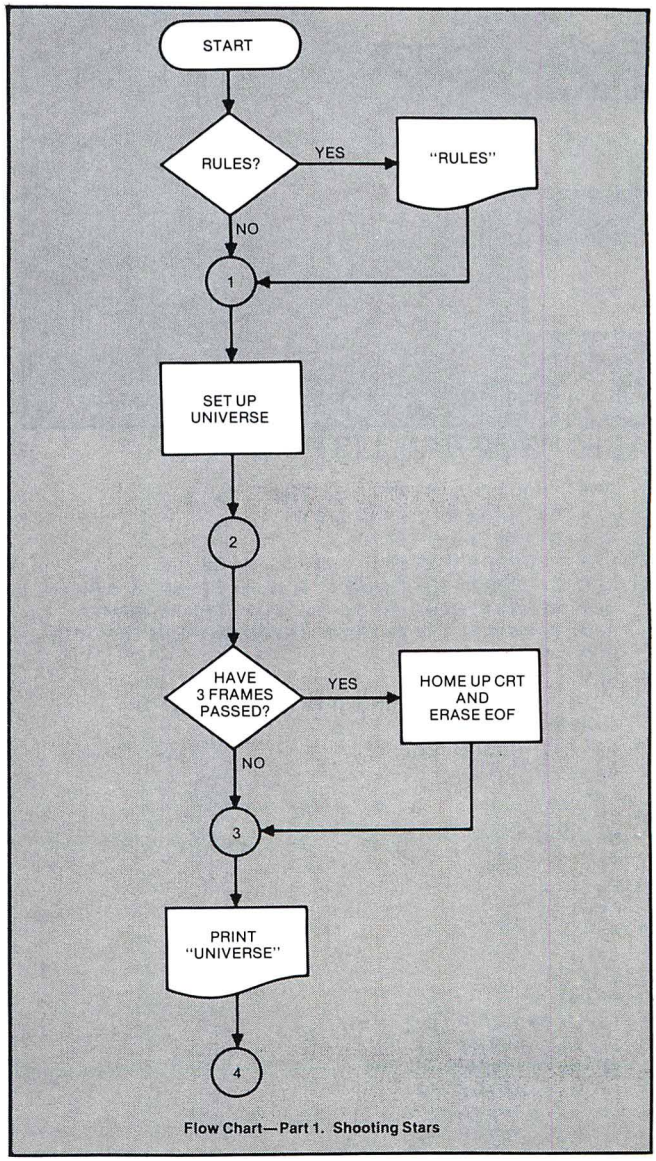
If you are running this on the TTY terminal, then there will be no use for the control statements used as cursor control. There are three sets of statements at the end of each instruction frame designed to hold that frame until the next one is wanted. These statements and the INPUT Z statements that follow will have no use with a TTY terminal.

RUNNING SHOOTING STARS WITH 4K MEMORY

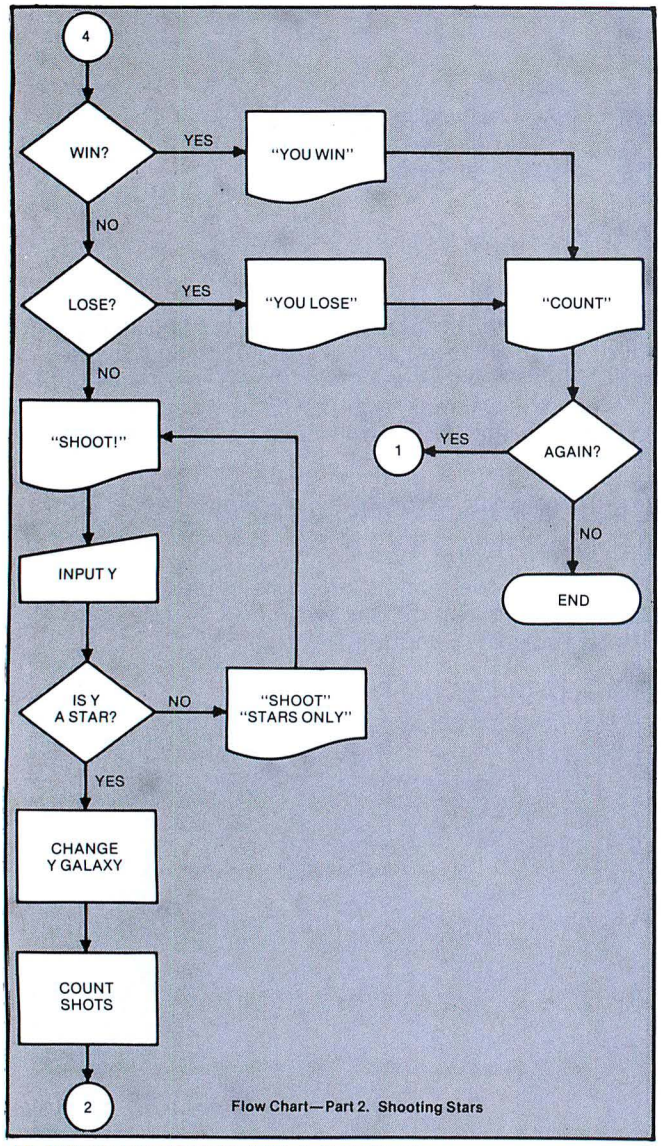
By removing the instructions, this could be run on a machine with only 4K of memory.

I hope you enjoy Shooting Stars.

PROGRAM FLOW DIAGRAM



Flow Chart—Part 1. Shooting Stars



Flow Chart—Part 2. Shooting Stars

BASIC PROGRAM LISTING

```
000 REM SHOOTING STARS IN TBX
001 REM BY HERMAN DEMONSTOY
002 REM DATE: 12-18-76
003 REM MICROCOMPUTER: SWTP'S 6800
004 REM SUPPORT SOFTWARE: TOM PITTMAN'S TBX
005 REM MEMORY REQUIRED: 2K FOR TBX & GAME
006 REM TERMINAL: CT-1024 KEYBOARD-CRT OR TTY
007 REM
008 REM
010 PRINT "INSTRUCTIONS (1=YES, 0=NO)";
020 INPUT Z
030 IF Z=1 GOSUB 900
100 A=-1
101 B=-1
102 C=-1
103 D=-1
104 E=1
105 F=-1
106 G=-1
107 H=-1
108 I=-1
109 J=0
148 PRINT
149 IF J/3*3=J PRINT "";
150 IF A=1 PRINT "* ";
151 IF A=-1 PRINT "- ";
155 IF B=1 PRINT "* ";
156 IF B=-1 PRINT "- ";
160 IF C=1 PRINT "*  ";J
161 IF C=-1 PRINT "-  ";J
165 IF D=1 PRINT "* ";
166 IF D=-1 PRINT "- ";
170 IF E=1 PRINT "* ";
171 IF E=-1 PRINT "- ";
175 IF F=1 PRINT "*"
176 IF F=-1 PRINT "-"
180 IF G=1 PRINT "* ";
181 IF G=-1 PRINT "- ";
185 IF H=1 PRINT "* ";
186 IF H=-1 PRINT "- ";
190 IF I=1 PRINT "*      ";
191 IF I=-1 PRINT "-      ";
250 IF E=1 GOTO 390
260 IF A+B+C+D+F+G+H+I=8 GOTO 809
270 IF A+B+C+D+F+G+H+I=-8 GOTO 820
390 PRINT "SHOOT";
391 INPUT Y
395 GOSUB 499+Y*10
397 J=J+1
400 GOTO 148
499 PRINT "YOU GAVE UP ON ";J;" TRYS !!!"
500 GOTO 830
509 IF A=-1 GOTO 800
510 A=-A
511 B=-B
512 D=-D
513 E=-E
516 RETURN
519 IF B=-1 GOTO 800
520 A=-A
521 B=-B
522 C=-C
526 RETURN
529 IF C=-1 GOTO 800
530 B=-B
531 C=-C
532 E=-E
533 F=-F
536 RETURN
539 IF D=-1 GOTO 800
540 A=-A
541 D=-D
542 G=-G
546 RETURN
549 IF E=-1 GOTO 800
550 B=-B
551 D=-D
552 E=-E
553 F=-F
554 H=-H
556 RETURN
559 IF F=-1 GOTO 800
560 C=-C
561 F=-F
562 I=-I
566 RETURN
569 IF G=-1 GOTO 800
570 D=-D
571 E=-E
572 G=-G
573 H=-H
576 RETURN
579 IF H=-1 GOTO 800
580 G=-G
581 H=-H
582 I=-I
586 RETURN
589 IF I=-1 GOTO 800
590 E=-E
591 F=-F
592 H=-H
593 I=-I
596 RETURN
599 RETURN
800 PRINT "HEY !! YOU CAN ONLY SHOOT"
801 PRINT "STARS, NOT BLACK HOLES."
802 GOTO 390
809 PRINT
```

DIODES/ZENERS

1N914	100v	10mA	.05
1N4004	400v	1A	.08
1N4005	600v	1A	.08
1N4007	1000v	1A	.15
1N4148	75v	10mA	.03
1N753A	6.2v	z	.25
1N758A	10v	z	.25
1N759A	12v	z	.25
1N4733	5.1v	z	.25
1N5243	13v	z	.25
1N5244B	14v	z	.25
1N5245B	15v	z	.25

SOCKETS/BRIDGES

8-pin	pcb	.25	ww	.45
14-pin	pcb	.25	ww	.40
16-pin	pcb	.25	ww	.40
18-pin	pcb	.25	ww	.75
22-pin	pcb	.45		
24-pin	pcb	.35	ww	1.25
28-pin	pcb	.35	ww	1.45
40-pin	pcb	.50	ww	1.95

Molex pins .01 To-3 Sockets .25

2 Amp Bridge 100-prv 1.20

25 Amp Bridge 200-prv 2.50

TRANSISTORS, LEDS, etc.

2N2222	NPN		.10
2N2907	PNP		.15
2N3740	PNP	1A 60v	.25
2N3906	PNP		.10
2N3055	NPN	15A 60v	.50
T1P125	PNP	Darlington	.35

LED Green, Red, Clear .15

D.L.747 7 seg 5/8" high com-anode 1.95

XAN72 7 seg com-anode 1.50

FND 359 Red 7 seg com-cathode 1.25

C MOS

4000	.20
4001	.20
4002	.25
4004	4.95
4006	1.20
4007	.40
4008	1.20
4009	.25
4010	.45
4011	.20
4012	.20
4013	.40
4014	1.10
4015	.95
4016	.35
4017	1.10
4018	1.10
4019	.70
4020	.85
4021	1.35
4022	1.15
4023	.25
4024	.75
4025	.35
4026	1.95
4027	.50
4028	.95
4030	.45
4033	1.95
4034	2.45
4035	1.25
4040	1.35
4041	.69
4042	.95
4043	1.25
4044	.95
4046	1.50
4049	.80
4050	.70
4066	1.35
4069	.40
4071	.35
4082	.45

— T T L —

7400	.15
7401	.15
7402	.20
7403	.25
7404	.15
7405	.25
7406	.35
7407	.55
7408	.25
7409	.15
7410	.15
7411	.25
7412	.30
7413	.65
7414	1.10
7416	.25
7417	.50
7420	.15
7426	.40
7427	.45
7430	.15
7432	.45
7437	.45
7438	.35
7440	.25
7441	1.15
7442	.65
7443	.95
7444	.55
7445	.95
7446	.95
7447	.95
7448	1.20
7450	.25
7451	.25
7453	.25
7454	.25
7460	.40
7470	.45
7472	.45
7473	.35
7474	.40
7475	.45
7476	.20
7480	.65
7481	.99
7483	1.00
7485	1.05
7486	.40
7489	2.50
7490	.55
7491	1.15
7492	.95
7493	.45
7494	1.25
7495	.85
7496	.95
74100	1.85
74107	.45
74121	.40
74122	.55
74123	.55
74125	.45
74132	1.35
74141	1.30
74150	1.00
74151	.95
74153	.95
74154	.75
74156	1.15
74157	.75
74161	1.25
74163	1.25
74164	.95
74165	1.50
74166	1.35
74175	.95
74176	1.25
74180	.85
74181	3.25
74182	.95
74190	1.75
74192	1.65
74193	.85
74194	1.45
74195	.95
74196	1.50
74197	1.25
74198	2.35
74367	.85
75108A	.35
75110	.35
75491	.50
75492	.50
74H00	.25
74H01	.25
74H04	.25
74H05	.25
74H11	.25
74H15	.30
74H20	.30
74H22	.40
74H30	.25
74H40	.25
74H51	.25
74H52	.15
74H53J	.25
74H55	.25
74H72	.55
74H101	.75
74H103	.75
74H106	.95
74L00	.35
74L02	.35
74L03	.30
74L10	.35
74L30	.45
74L47	1.95
74L55	.65
74L72	.45
74L75	.55
74S00	.55
74S02	.55
74S03	.50
74S04	.45
74S05	.45
74S08	.45
74S10	.45
74S11	.45
74S20	.50
74S40	.30
74S50	.35
74S51	.45
74S64	.30
74S74	.50
74S112	1.50
74S133	.45
74S140	.75
74S151A	.45
74S153	.45
74S158	.45
74S194	1.50
74S257 (8123)	.25
74LS00	.45
74LS01	.45
74LS02	.45
74LS04	.55
74LS08	.45
74LS09	.45
74LS10	.45
74LS11	.45
74LS20	.50
74LS21	.25
74LS22	.25
74LS32	.55
74LS37	.40
74LS40	.55
74LS42	1.75
74LS74	.95
74LS90	1.30
74LS93	1.00
74LS107	.95
74LS153	1.20
74LS157	.85
74LS164	1.90
74LS367	.85
74LS368	.70

9000 SERIES

9301	1.00
9309	.45
9322	1.10
9602	1.50

MEMORY, CLOCKS

74S188(8223)	3.00
MM1702A	9.95
MM5314	3.50
MM5316	3.95
2102-1	1.75
TR 1602A	6.95
TMS6011NC	6.95
8080AD	19.50
8T23	1.50
8T24	2.00
2107B-4	5.95

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MCT2	.95
8038	3.95
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LM301AH	.25
LM308AH	1.00
LM309H	.65
LM309K	.90
LM310	1.15
LM311D (Mini)	.95
LM320K5	1.65
LM320K12	1.65
LM320T12	1.65
LM320T15	1.65
LM339	.95
7805(340T-5)	1.00
LM340T-12	1.25
LM340T-15	1.25
LM340T-18	1.65
LM340T-24	1.25
LM340K-12	2.15
LM340K-15	1.65
LM340K-18	1.65
LM340K-24	1.25
LM373	2.95
LM380	.95
LM709 (8, 14 PIN)	.30
LM711	.45
LM723	.45
LM725	1.95
LM739	1.50
LM741 8-14	.25
LM747	1.10
LM1307	1.25
LM1458	.95
LM3900	.65
LM75451	.65
NE555	.50
NE556	1.10
NE565	.95
NE566	1.75
NE567	1.35
SN72720	.35
SN72820	.35

```
810 PRINT "YOU WON WITH ";J;" SHOTS"
815 GOTO 830
820 PRINT "YOU LOST WITH ";J;" TRYS."
830 PRINT
831 PRINT "TRY AGAIN (1=YES, 0=NO)";
832 INPUT X
833 IF X=1 GOTO 100
834 IF X=0 GOTO 890
835 PRINT "FOLLOW INSTRUCTIONS "
836 GOTO 831
890 PRINT "HOPE YOU HAD FUN"
895 END
899 REM INSTRUCTION SUBROUTINE
900 PRINT "";
901 PRINT "* * *  THERE ARE STARS"
902 PRINT "- - -  AND BLACK HOLES"
903 PRINT "* * *  IN THE UNIVERSE"
904 PRINT
905 PRINT "1 2 3  YOU SHOOT A STAR *"
906 PRINT "4 5 6  NOT A BLACK HOLE -"
907 PRINT "7 8 9  BY TYPING ITS NUMBER"
908 PRINT
910 PRINT "EACH STAR IS IN A GALAXY."
911 PRINT "WHEN YOU SHOOT A STAR, EVERY-"
912 PRINT "THING IN ITS GALAXY CHANGES."
913 PRINT "ALL STARS BECOME BLACK HOLES,"
914 PRINT "ALL BLACK HOLES BECOME STARS."
915 PRINT "TYPE '2' TO GO ON.";
916 INPUT Z
920 PRINT "GALAXY MAPS:"
921 PRINT
923 PRINT "1 * -  * 2 *  - * 3"
924 PRINT "* * -  - - -  - * *"
925 PRINT "- - -  - - -  - - -"
926 PRINT
927 PRINT "* - -  - * -  - - *"
928 PRINT "4 - -  * 5 *  - - 6"
929 PRINT "* - -  - * -  - - *"
930 PRINT
931 PRINT "- - -  - - -  - - -"
932 PRINT "* * -  - - -  - * *"
933 PRINT "7 * -  * 8 *  - * 9"
934 PRINT
935 PRINT "TYPE '3' TO GO ON";
936 INPUT Z
940 PRINT "PATTERNS TO LOOK FOR:"
941 PRINT
942 PRINT "START      WIN      LOSE"
943 PRINT
945 PRINT "- - -     * * *     - - -"
946 PRINT "- * -     * - *     - - -"
947 PRINT "- - -     * * *     - - -"
948 PRINT
949 PRINT "TYPE '0' TO END GAME"
950 PRINT
951 PRINT "TYPE '4' TO GO ON";
952 INPUT Z
999 RETURN
1000 END
```

```
 RUN
INSTRUCTIONS (1=YES, 0=NO)? 0

- - -  0
- * -
- - -      SHOOT? 5

- * -  1
* - *
- * -      SHOOT? 2

* - *  2
* - *
- * -      SHOOT? 8

* - *  3
* - *
* - *      SHOOT? 1

- * *  4
- * *
* - *      SHOOT? 9

- * *  5
- - -
* * -      SHOOT? 3

- - -  6
- * *
* * -      SHOOT? 5

- * -  7
* - -
* - -      SHOOT? 7

- * -  8
- * -
- * -      SHOOT? 2

* - *  9
- * -
- * -      SHOOT? 8

* - *  10
- * -
* - *      SHOOT? 5

* * *  11
* - *
* * *
YOU WON WITH 11 SHOTS

TRY AGAIN (1=YES, 0=NO)? 0
HOPE YOU HAD FUN

:
```

EXMON-6800 Extended Monitor System

By Michael Burton

INTRODUCTION

EXMON, the EXtended MONitor system, is a software extension of the MIKBUG (R) (Motorola) firmware monitor system. EXMON fills in some deficient areas of MIKBUG (R) by implementing ten new commands and by upgrading the P and G commands. The other standard MIKBUG (R) commands (M, L and R) are also recognized by EXMON and are implemented by going to the appropriate MIKBUG (R) routine. All EXMON functions except G terminate either to EXMON or MIKBUG (R). are explained below.

EXTENDED MONITOR COMMANDS

The new and upgraded commands are;

P XXX YYYY —Upgraded MIKBUG (R) command. Punch/list data from address XXXX to YYYY. An innitial cassette recorder motor start up delay is provided. This command returns control to MIKBUG (R) upon completion.

G XXXX —Upgraded MIKBUG (R) command. Load the A, B, X and CC registers from the users stack and go to the users program at address XXXX.

A HH XX —Display and/or change the A register contained in the users stack. EXMON outputs the register contents HH and then solicits an input XX. If the input is hexadecimal, the register is changed and EXMON retains control. If a non-hexadecimal input is made, the register is not changed and control returns to MIKBUG (R).

B HH XX —Display and/or change the B register. Works the same as (A) above.

C HH XX —Display and/or change the condition codes register. Works the same as (A) above.

X HHHH XXXX —Display and/or change the index register. Works the same as (A) above.

S XXXX ABCDE . . . —Being with address XXXX, enter the ASCII string ABCDE . . . into consecutive memory locations. The string is terminated with an end-of-tape character (control D) which is also placed in memory. EXMON retains control following the EOT.

I XXXX YYYY ZZ —Place the hexadecimal value ZZ into consecutive memory locations from address XXXX to YYYY. This command returns control to EXMON.

E XXXX WW YY ZZ . . . —Beginning with address XXXX, enter hexadecimal data WW YY ZZ . . . into consecutive memory locations. Data entry is terminated with a non-hexadecimal character. Control is returned to MIKBUG (R).

T XXXX YYYY —Put a software interrupt instruction (3F) at address XXXX, load the registers from the users stack and begin execution of the users program at address YYYY. When the software interrupt instruction is encountered, program execution is interrupted and control returns to MIKBUG (R), which prints the registers' contents.

F XXXX YYYY ZZ —Between addresses XXXX and YYYY, print all addresses containing the hexadecimal value ZZ. EXMON retains control following execution of this command.

D XXXX YYYY —Between addresses XXXX and YYYY, print the contents of memory on the serial control device. EXMON retains control following execution of this command.

EXMON MEMORY REQUIREMENTS

EXMON requires 387 bytes of memory. It was assembled at 1E00, which is the beginning of the upper 512 bytes of an 8K system. If you wish to relocate EXMON, there are 14 instructions whose operands must be changed, as they use the extended addressing mode. The changes are as follows:

1. Determine the new EXMON starting address (s.a.)
2. On the listing, change

   1E04 and 1E05 to be s.a. plus 17B
   1EC5 and 1³C6 to be s.a.
   1ED3 and 1ED4 to be s.a. plus 17A
   1EDB and 1EDC to be s.a. plus 17A
   1EFF and 1FOO to be s.a. plus 17A
   1F02 and 1F03 to be s.a. plus 18O
   1F14 and 1F15 to be s.a. plus 17A
   1F23 and 1F24 to be s.a. plus 17A
   1F2B and 1F2C to be s.a. plus 17A
   1F33 and 1F34 to be s.a. plus 180
   1F55 and 1F56 to be s.a. plus 180
   1F5C and 1F5D to be s.a. plus 17A
   1F67 and 1F68 to be s.a. plus E7
   1F74 and 1F75 to be s.a. plus 17A

EXMON may now be entered beginning at the new starting address.

RUNNING EXMON

Sample EXMON output, the EXMON assembly listing and a Motorola 'S' format dump of the program is shown below.

SAMPLE EXMON OUTPUT

```
*G
:A C1 01                          (Change A reg.)
:B OF .                           (Change A reg.)
*G                                (Display B reg.)
:C E1 FF                          (Change CC reg.)
:X D1EC 0000                      (Change X reg.)
:R FF OF 01 oooo iE00 A042        (Display all registers)
*G
:S 000                            (ASCII string entry)
THIS IS AN ASCII TEST STRING.
:E 0100                           (Hexadecimal data entry)
 CE 00 00 BD EO 7E 7E 1E
 00 .
*G
:G 0100                           (Go to a users program)
THIS IS AN ASCII TEST STRING.
:F 0000 001D 41                   (Find all ASCII A's in string)
0008
000B
:D 0100 0108                      (Dump the user program)
0100 CE 00 00 BD EO 7E 7E 1E
0108 00
:T 0106 0100                      (SWI after string output)
THIS IS AN ASCII TEST STRING.E1 DC 04 001E 0106 A042
 *M a048                          (Reset P reg. to EXMON)
 *A048 01     1E
 *A049 06     00
 *A04a C9
*G
:P A068 A06F                      (Record a memory section)
S10BA068E6F6A070B6A0713900
*G
:I 0200 0300 3F                   (Initialize memory to SWIs)
:L                                (Load program)
*G
:M A048                           (Memory display change)
*A048 1E .
*
```

ASSEMBLY PROGRAM LISTING

```
00001                    NAM    EXMON
00002                *   PROGRAM NAME: EXMON-EXTENDED MIKBUG(R) MONITOR.
00003                *   PROGRAMMER: MICHAEL BURTON
00004                *   MICROCOMPUTER: SWTPC 6800
00005                *   INTERFACE EQUIPMENT: CT1024 WITH AC-30
00006                *
00007                *   NORMAL MIKBUG(R) COMMANDS ARE M, L, P, R AND G.
00008                *   THE P AND G COMMANDS ARE CHANGED AS DETAILED
00009                *   BELOW.
00010                *   P XXXX YYYY     - PUNCH/LIST FROM ADDR. XXXX TO
00011                *                     ADDR. YYYY.  CASSETTE START UP
00012                *                     DELAY IS BUILT IN.
00013                *   G XXXX          - GO TO USERS PROGRAM AT XXXX.
00014                *
00015                *   A               - DISPLAY/CHANGE A REG CONTENTS.
00016                *   B               - DISPLAY/CHANGE B REG CONTENTS.
00017                *   C               - DISPLAY/CHANGE CC REG CONTENTS.
00018                *   X               - DISPLAY/CHANGE X REG CONTENTS.
00019                *   S XXXX ABCDE... - STARTING AT ADDRESS XXXX, ENTER
00020                *                     ASCII STRING ABCDE... TERMINATE
00021                *                     WITH A CONTROL D(04).
00022                *   I XXXX YYYY ZZ  - INITIALIZE LOCATIONS XXXX THRU
00023                *                     YYYY TO VALUE ZZ.
00024                *   E XXXX WW YY.... - ENTER HEX DATA BEGINNING AT
00025                *                     XXXX.  TERMINATE WITH A C/R.
00026                *   T XXXX YYYY     - PUT A SOFTWARE INTERRUPT AT
00027                *                     XXXX AND BEGIN EXECUTION AT
00028                *                     YYYY.
00029                *   F XXXX YYYY ZZ  - BETWEEN XXXX AND YYYY, FIND
00030                *                     AND PRINT LOCATIONS OF VALUE ZZ.
00031                *   D XXXX YYYY     - DUMP XXXX TO YYYY ON THE SERIAL
00032                *                     CONTROL DEVICE.
00033                *
00034 1E00                   ORG    $1E00
00035      E078      INCH    EQU    $E078
00036      E085      CHANGE  EQU    $E085
```

```
00037        E11F    PRINT   EQU     $E11F
00038        E00A    LOAD    EQU     $E00A
00039        E13D    PUNCH   EQU     $E13D
00040        E1D1    OUTEEE  EQU     $E1D1
00041        A00C    XHI     EQU     $A00C
00042        A008    SP      EQU     $A008
00043        A002    BEGA    EQU     $A002
00044        A004    ENDA    EQU     $A004
00045                *
00046                        OPT     SYMBOLS
00047        1E00    EXMON   EQU     *
00048 1E00 8E A042           LDS     #$A042  SET STACK POINTER
00049 1E03 CE 1F7B           LDX     #PROMPT
00050 1E06 8D 7B             BSR     PDATA1  PRINT PROMPT
00051 1E08 BD E078           JSR     INCH    GET COMMAND
00052 1E0B 16                TAB
00053 1E0C 8D 78             BSR     OUTS    PRINT A SPACE
00054 1E0E C1 4D             CMP B   #'M     MEMORY CHANGE?
00055 1E10 26 03             BNE     CHKL    NO.
00056 1E12 7E E085           JMP     CHANGE  YES.
00057 1E15 C1 4C    CHKL     CMP B   #'L     LOAD TAPE?
00058 1E17 26 03             BNE     CHKR    NO.
00059 1E19 7E E00A           JMP     LOAD    YES.
00060 1E1C C1 52    CHKR     CMP B   #'R     REGISTER DISPLAY?
00061 1E1E 26 03             BNE     CHKP    NO.
00062 1E20 7E E11F           JMP     PRINT   YES.
00063 1E23 C1 50    CHKP     CMP B   #'P     PUNCH(RECORD) TAPE?
00064 1E25 26 1C             BNE     CHKG    NO.
00065 1E27 8D 77             BSR     LIMITS  GET LIMITS.
00066 1E29 FE A004           LDX     ENDA
00067 1E2C 09                DEX
00068 1E2D FF A004           STX     ENDA
00069 1E30 86 12             LDA A   #$12
00070 1E32 BD E1D1           JSR     OUTEEE  SEND RECORD ON.
00071 1E35 CE 04FF           LDX     #$4FF   .INITIATE
00072 1E38 86 FF    DLP1     LDA A   #$FF    ..CASSETTE
00073 1E3A 4A       DLP2     DEC A           ...DELAY
00074 1E3B 26 FD             BNE     DLP2
00075 1E3D 09                DEX
00076 1E3E 26 F8             BNE     DLP1
00077 1E40 7E E13D           JMP     PUNCH   THEN GO PUNCH
00078 1E43 C1 47    CHKG     CMP B   #'G     GOTO USER?
00079 1E45 26 13             BNE     CHKT    NO.
00080 1E47 8D 67    GOTO     BSR     BADDR   YES. GET ADDR
00081 1E49 FE A008           LDX     SP      GET USER STACK PNTR.
00082 1E4C B6 A00C           LDA A   XHI     GET UPPER BYTE OF ADDR.
00083 1E4F A7 06             STA A   6,X     PUT IN P-REG.
00084 1E51 B6 A00D           LDA A   XHI+1   GET LOWER BYTE OF ADDR.
00085 1E54 A7 07             STA A   7,X     PUT IN P-REG.
00086 1E56 BE A008           LDS     SP      LOAD USER STACK PNTR.
00087 1E59 3B                RTI             GO TO USER.
00088 1E5A C1 54    CHKT     CMP B   #'T     TRAP?
00089 1E5C 26 0A             BNE     CHKA    NO.
00090 1E5E 8D 50             BSR     BADDR   GET INTERRUPT ADDR.
00091 1E60 86 3F             LDA A   #$3F
00092 1E62 A7 00             STA A   0,X     STORE SWI AT I.A.
00093 1E64 8D 20             BSR     OUTS    SPACE
00094 1E66 20 DF             BRA     GOTO
00095 1E68 FE A008 CHKA      LDX     SP      GET USER STACK PNTR.
00096 1E6B 08                INX
00097 1E6C C1 41             CMP B   #'A     A REG DISP/CHG?
00098 1E6E 27 0A             BEQ     RDC     YES.
00099 1E70 08                INX
00100 1E71 C1 42             CMP B   #'B     B REG DISP/CHG?
00101 1E73 27 05             BEQ     RDC     YES.
00102 1E75 08                INX
00103 1E76 C1 43             CMP B   #'C     CC REG DISP/CHG?
00104 1E78 26 0F             BNE     CHKX    NO.
00105 1E7A 8D 6B    RDC      BSR     OUT2HS  OUTPUT REG CONTENTS
00106 1E7C 09                DEX
00107 1E7D 8D 6E             BSR     BYTE    GET NEW CONTENTS
00108 1E7F A7 00             STA A   0,X     AND STORE IN USER STACK
00109 1E81 20 41             BRA     RET     GO BACK
00110 1E83 7E E07E PDATA1    JMP     $E07E   PRINT ASCII STRING
00111 1E86 7E E0CC OUTS      JMP     $E0CC   PRINT SPACE
00112 1E89 C1 58    CHKX     CMP B   #'X     X REG DISP/CHG?
00113 1E8B 26 26             BNE     CHKS    NO.
00114 1E8D 8D 5B             BSR     OUT4HS  OUTPUT X REG CONTENTS
00115 1E8F 8D 1F             BSR     BADDR   GET NEW CONTENTS
00116 1E91 FE A008           LDX     SP      GET USER STACK PNTR.
00117 1E94 B6 A00C           LDA A   XHI     GET UPPER BYTE
00118 1E97 A7 04             STA A   4,X     STORE IN X REG
00119 1E99 B6 A00D           LDA A   XHI+1   GET LOWER BYTE
00120 1E9C A7 05             STA A   5,X
00121 1E9E 20 24             BRA     RET     GO BACK
00122 1EA0 8D 0E    LIMITS   BSR     BADDR   GET LOWER ADDR
00123 1EA2 FF A002           STX     BEGA    STORE IT
00124 1EA5 8D DF             BSR     OUTS    SPACE
00125 1EA7 8D 07             BSR     BADDR   GET UPPER ADDR
00126 1EA9 08                INX
00127 1EAA FF A004           STX     ENDA    STORE IT
00128 1EAD 8D D7             BSR     OUTS    SPACE
00129 1EAF 39                RTS
00130 1EB0 7E E047 BADDR     JMP     $E047   BUILD 3 BYTES
00131 1EB3 C1 53    CHKS     CMP B   #'S     ASCII INPUT?
00132 1EB5 26 13             BNE     CHKI    NO.
00133 1EB7 8D F7             BSR     BADDR   GET ADDR.
00134 1EB9 8D CB             BSR     OUTS    SPACE
00135 1EBB BD E078 ASCLOP    JSR     INCH    GET A CHARACTER.
00136 1EBE A7 00             STA A   0,X     STORE IT.
00137 1EC0 81 04             CMP A   #$04    EOT?
00138 1EC2 26 03             BNE     ASCCNT  NO.
00139 1EC4 7E 1E00 RET       JMP     EXMON   YES. RETURN.
00140 1EC7 08        ASCCNT  INX
00141 1EC8 20 F1             BRA     ASCLOP
00142 1ECA C1 49    CHKI     CMP B   #'I     INITIALIZE MEMORY?
00143 1ECC 26 28             BNE     CHKE    NO.
00144 1ECE 8D D0             BSR     LIMITS  GET LIMITS
00145 1ED0 8D 1B             BSR     BYTE    GET INIT BYTE
00146 1ED2 B7 1F7A           STA A   TEMP
00147 1ED5 8D AF             BSR     OUTS    SPACE
00148 1ED7 FE A002           LDX     BEGA
00149 1EDA B6 1F7A           LDA A   TEMP
00150 1EDD A7 00    IMLOOP   STA A   0,X     STORE INIT BYTE
00151 1EDF 08                INX
00152 1EE0 BC A004           CPX     ENDA    LAST CELL TO INIT?
00153 1EE3 26 F8             BNE     IMLOOP  NO.
00154 1EE5 20 DD    RET1     BRA     RET     YES. GO BACK.
00155 1EE7 7E E0CA OUT2HS    JMP     $E0CA   PRINT BYTE + SPACE
00156 1EEA 7E E0C8 OUT4HS    JMP     $E0C8   PRINT 2 BYTES + SPACE
00157 1EED 7E E055 BYTE      JMP     $E055   INPUT A BYTE
00158 1EF0 20 91    PDT1     BRA     PDATA1
00159 1EF2 20 92    OTS      BRA     OUTS
00160 1EF4 20 AA    LMTS     BRA     LIMITS
00161 1EF6 C1 45    CHKE     CMP B   #'E     HEX DATA ENTRY?
00162 1EF8 26 20             BNE     CHKF    NO.
00163 1EFA 8D B4             BSR     BADDR   GET ADDR.
00164 1EFC 86 08    NWLN     LDA A   #$8
00165 1EFE B7 1F7A           STA A   TEMP
00166 1F01 CE 1F80           LDX     #CRLF
00167 1F04 8D EA             BSR     PDT1
00168 1F06 FE A00C           LDX     XHI
00169 1F09 8D E7    HEXLOP   BSR     OTS     SPACE
00170 1F0B 8D E0             BSR     BYTE    GET INPUT
00171 1F0D A7 00             STA A   0,X     STORE IT
00172 1F0F 08                INX
00173 1F10 FF A00C           STX     XHI
00174 1F13 7A 1F7A           DEC     TEMP
00175 1F16 27 E4             BEQ     NWLN
00176 1F18 20 EF             BRA     HEXLOP  NOT DONE.
00177 1F1A C1 46    CHKF     CMP B   #'F     FIND?
00178 1F1C 26 29             BNE     CHKD    NO.
00179 1F1E 8D D4             BSR     LMTS
00180 1F20 8D CB             BSR     BYTE    GET FIND BYTE
00181 1F22 B7 1F7A           STA A   TEMP
00182 1F25 FE A002           LDX     BEGA
00183 1F28 A6 00    FLOOP    LDA A   0,X     GET A BYTE
00184 1F2A B1 1F7A           CMP A   TEMP    SAME AS FIND?
00185 1F2D 26 10             BNE     FCONT   NO.
00186 1F2F FF A002           STX     BEGA
00187 1F32 CE 1F80           LDX     #CRLF
00188 1F35 8D B9             BSR     PDT1    DO A C/R L/F
00189 1F37 CE A002           LDX     #BEGA
00190 1F3A 8D AE             BSR     OUT4HS  PRINT FOUND BYTE
00191 1F3C FE A002           LDX     BEGA
00192 1F3F 08        FCONT   INX
00193 1F40 BC A004           CPX     ENDA    LAST FIND CELL?
00194 1F43 26 E3             BNE     FLOOP   NO.
00195 1F45 20 9E    RET2     BRA     RET1
00196 1F47 C1 44    CHKD     CMP B   #'D     DUMP?
00197 1F49 26 9A             BNE     RET1
00198 1F4B 8D A7             BSR     LMTS    YES.
00199 1F4D FE A004           LDX     ENDA
00200 1F50 09                DEX
00201 1F51 FF A004           STX     ENDA
00202 1F54 CE 1F80 DLOOP     LDX     #CRLF
00203 1F57 8D 97             BSR     PDT1    OUTPUT A C/R L/F
00204 1F59 86 08             LDA A   #$8
00205 1F5B B7 1F7A           STA A   TEMP    INIT LINE COUNTER.
00206 1F5E CE A002           LDX     #BEGA
00207 1F61 8D 87             BSR     OUT4HS  OUTPUT ADDR
00208 1F63 FE A002 DLOOPI    LDX     BEGA
00209 1F66 BD 1EE7           JSR     OUT2HS  OUTPUT BYTE
00210 1F69 09                DEX
00211 1F6A BC A004           CPX     ENDA    LAST BYTE TO DUMP?
00212 1F6D 27 D6             BEQ     RET2    YES.
00213 1F6F 08                INX
00214 1F70 FF A002           STX     BEGA
00215 1F73 7A 1F7A           DEC     TEMP    DECREMENT LINE COUNT
00216 1F76 26 EB             BNE     DLOOPI  DONE WITH LINE?
00217 1F78 20 DA             BRA     DLOOP   YES.
00218 1F7A 0001     TEMP     RMB     1
00219 1F7B 0D       PROMPT   FCB     $0D,$0A,$15,$3A,$04
      1F7C 0A
      1F7D 15
      1F7E 3A
      1F7F 04
00220 1F80 0D       CRLF     FCB     $0D,$0A,$15,$04
      1F81 0A
      1F82 15
      1F83 04
00221                        END
INCH    E078
CHANGE E085   PRINT   E11F   LOAD    E00A   PUNCH   E13D   OUTEEE E1D1
XHI     A00C  SP      A008   BEGA    A002   ENDA    A004   EXMON  1E00
CHKL    1E15  CHKR    1E1C   CHKP    1E23   DLP1    1E38   DLP2   1E3A
CHKG    1E43  GOTO    1E47   CHKT    1E5A   CHKA    1E68   RDC    1E7A
PDATA1  1E83  OUTS    1E86   CHKX    1E89   LIMITS  1EA0   BADDR  1EB0
CHKS    1EB3  ASCLOP 1EBB   RET     1EC4   ASCCNT  1EC7   CHKI   1ECA
IMLOOP  1EDD  RET1    1EE5   OUT2HS  1EE7   OUT4HS  1EEA   BYTE   1EED
PDT1    1EF0  OTS     1EF2   LMTS    1EF4   CHKE    1EF6   NWLN   1EFC
HEXLOP  1F09  CHKF    1F1A   FLOOP   1F28   FCONT   1F3F   RET2   1F45
CHKD    1F47  DLOOP   1F54   DLOOPI  1F63   TEMP    1F7A   PROMPT 1F7B
CRLF    1F80
TOTAL ERRORS 00000
```

OBJECT CODE LISTING

```
S1131E008EA042CE1F7B8D7BBDE07816BD78C14DB0
S1131E1026037EE085C14C26037EE00AC1522603D8
S1131E207EE11FC150261C8D77FEA00409FFA0048B
S1131E308612BDE1D1CE04FF86FF4A26FD0926F8AD
S1131E407EE13DC1472613BD67FEA008B6A00CA70E
S1131E5006B6A00DA707BEA0083BC154260A8D50A4
S1131E60863FA7008D2020DFFEA00808C141270A75
S1131E7008C142270508C143260F8D6B098D6EA743
S1131E800020417EE07E7EE0CCC15826268D5B8D0D
S1131E901FFEA008B6A00CA704B6A00DA705202419
S1131EA08D0EFFA0028DDF8D0708FFA0048DD739AA
S1131EB07EE047C153261 38DF78DCBBDE078A70094
S1131EC0810426037E1E000820F1C14926288DD0F6
S1131ED08D1BB71F7A8DAFFEA002B61F7AA700082C
S1131EE0BCA00426F820DD7EE0CA7EE0C87EE05572
S1131EF0209120922 0AAC14526208DB48608B71FC0
S1131F007ACE1F808DEAFEA00C8DE78DE0A7000835
S1131F10FFA00C7A1F7A27E420EFC1462629 8DD42E
S1131F208DCBB71F7AFEA002A600B11F7A2610FF40
S1131F30A002CE1F808DB9CEA0028DAEFEA00208F5
S1131F40BCA00426E3209EC144269A8DA7FEA004CB
S1131F5009FFA004CE1F808D97860 8B71F7ACEA0F4
S1131F60028D87FEA002BD1EE709BCA00427D60887
S1131F70FFA0027A1F7A26EB20DAFE0D0A153A0436
S1071F800D0A150429

S105A0481E00F4
S9
```

PROPOSED CASSETTE DATA STORAGE FORMAT STANDARD

By Lorin S. Mohler
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INTRODUCTION

I have been in the process of putting together my own microprocessor system over the past year. During that time, my only I/O storage has been a paper tape system which has been very satisfactory but initially quite expensive. It now seems that most people are acquiring a cassette interface of one variety or another along with a cassette recorder, all at very reasonable prices. However, one giant problem has arisen. Everyone seems to have his own format from both the hardware and data standpoints. After much consideration, and effort, I have developed what I propose is a data format standard which will make most programmers happy. It has something for everyone.

ONE FORMAT FOR ALL TYPES OF DATA

Basically there is one format for all types of data, be it ASCII files, raw data, object code, etc. It has header self-checking capabilities, cyclic redundant check for the data record, single or multiple records, versatility for the record length, and number of records. It also has distinctive audio tones for records, file marks, and tape marks for audible listening locatability.

CRC

The cyclic redundant check (CRC) is used since it is capable of detecting errors associated with this method of data recording that the simple checksum cannot. The polynomial used to generate the CRC word is capable of handling the entire 64K memory as one record; however, this length of record is not recommended.

PROPOSED FORMAT DESIGNED FOR VERSATILITY

The proposed data format standard was designed only with versatility in mind, not for a particular cassette interface nor a particular microprocessor. Upon close examination, it might appear to lean toward one of the more popular microprocessors, but that was not the intention.

SUMMARY OF SECTIONS

Section I describes in detail the proposed cassette data format standard.

Section II describes one implementation of a Cassette Operating System, COS, for the proposed standard for saving and loading files. Remember that the proposed standard is what should be considered. The COS implementation demonstrates that the proposed standard works and how versatile it can be. Fully operational software is now available for the Intel 8080 microprocessor and the Tarbell cassette interface to save or load files based on the described implementation in Section II.

Section II also contains simplified flow charts and a source listing for the cassette routines. The command and parameter conversion routines are not presented as there are many acceptable methods of preparing the required buffers for each command.

COS MEMORY REQUIREMENTS

Although this implementation requires a total of approximately 680H bytes, it includes a large percentage of extremely flexible and expandable operating system. The file saving and loading routines take approximately 200H bytes. The intention, for the hobbyist with a minimal system, is to use a short checksum block loaded to load the more sophisticated cassette file save and load routines from cassette.

COS CAN BE EXPANDED

For those with PROM, the routines could be "burned-in" and available at "power on." The present software could easily be expanded to contain automatic drive start and stop commands with appropriate delays, multiple cassette capability, etc.

A source listing for the complete stand alone operating system and object paper tape, ORGed at 0, is available for $10. Source and object code on one cassette tape is also available for $15 + 6% California State Sales Tax. Copies of these programs are available from LSM Engineering, P.O. Box 3243, Orange, Calif. 92665 or 219 N. Sweetwater St., Anaheim, CA 92806.

SECTION I — PROPOSED CASSETTE STORAGE FORMAT STANDARD

TAPE RECORDING FORMAT

The proposed cassette recording format standard consists of the following type of recorded information segments;

- RECORD
- END OF FILE (EOF) MARK
- INTER RECORD GAP (IRG)
- GAP TO END OF TAPE (GEOT) MARK
- END OF TAPE (EOT) MARK

RECORDS

Records consist of a Record Header, Data and CRC information. For reference refer to figures 1 Record Format, 2 File Mark Format & 3 Tape Mark Format during the following discussion on tape recording format.

RECORD HEADER — Record Header information consist of a single ASCII record character Identifier, an eight printable ASCII character file name, a single ASCII File Type character, a two binary byte Record Number, a two binary byte Record Length, a two binary byte Load Start Address from one to 64K bytes of Data, and a two binary byte CRC. This Record Header information is recorded as 16 true/complement data pairs, totalling 32 bytes of information facilitating immediate error detection. This same basic header format is used for memory image data or text files reducing software requirements. Header ASCII characters are recorded with zero parity while the header binary numbers use all eight bits to represent binary numbers.

RECORD MARK IDENTIFIER—Single ASCII Character R

The Record Mark Identifier character R defines record type of information and provides direct differentiation between record, End of File Mark and End of Tape Mark type of recorded information.

FILE NAME — Up to Eight ASCII Characters

Provision for up to eight printable ASCII characters, header justified, of user defined file name. Prohibition of imbedded or trailing spaces prevents name abiguities. Null characters for remaining unused character positions indicates end of name.

FILE TYPE — Single ASCII Character

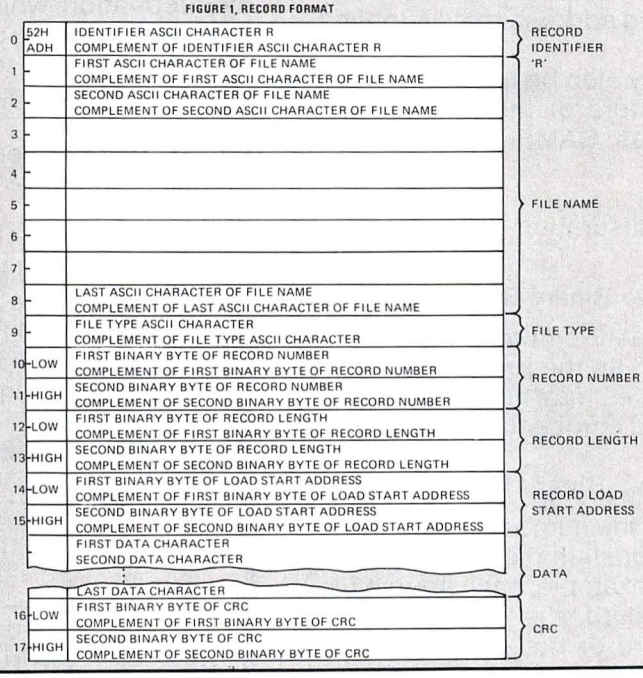
File Type identifies source of data load address to be used by COS and defines type of file data content. Five file Type characters are defined as follows;

I — Memory Image File in object code — Direct load uses load starting address contained in load start address location of header.

R — Relocatable File in object code — Indirect load requires load starting address to be supplied by calling program.

A — ASCII Text File — Indirect load requires load

FIGURE 1, RECORD FORMAT



starting address to be supplied by calling program.

B — BASIC program in ASCII — Indirect load requires load starting address to be supplied by calling program.

F — FORTRAN program in ASCII — Indirect load requires load starting address to be supplied by calling program.

Note: The File Name may also be used to contain additional descriptors of the File Type, if necessary, such as GAME 1:F A Fortran source file
XYZ: B A Basic file
and is left to the discretion of one naming the file.

RECORD NUMBER — Two Binary Bytes (0-FFFFH)

Record Number defines the number of a given file record with zero used as the first record number of a complete file. Files may be any combination of Record Length and number of records.

RECORD LENGTH — Two Binary Bytes (0-FFFH)

Record Length defines the number of data bytes of a given record. Files consisting of mixed record lengths are allowed. For example, each source file text line may be one record, the entire memory image may be one record or the entire memory image may be broken up into many short equal or unequal length records.

LOAD START — Two Binary Bytes (0-FFFFH)

Load Start defines the start of memory address of record and must be specified for direct loading to cassette tape storage from RAM memory (File Type I). Load Start address must be zero for non direct loading files (File Types R, A, B & F), such as text files. Calling program must specify the load Start address location for indirect load type files.

DATA—Up to 64K Bytes

Data may be true binary or ASCII Hex with or without parity as required by file type or usage. Files may consist of one to 64K bytes of data.

CRC—Two Binary bytes (O-FFFFH)

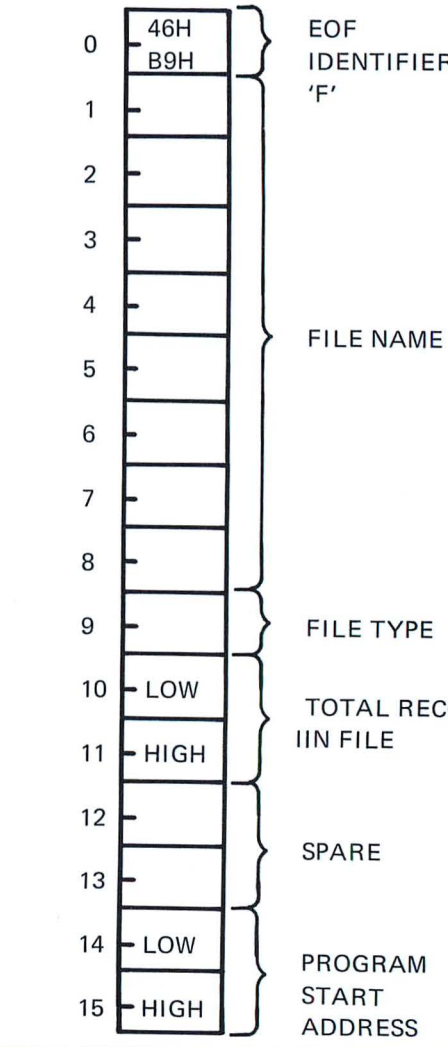
A Cyclic Redundant Check, CRC, of data bytes is recorded as two true/complement data pairs and is based on the polynomial $X^{16} + X^{12} + X^5 + 1$. CRC is initialized to **0FFFFH**, at the start of a load or read record command operation.

END OF FILE (EOF) MARK

EOF Mark identifies the end of file and is recorded only after the record gap following the last record of the file. EOF Mark information consists of a single ASCII character End of File Identifier, an eight printable ASCII character File Name, a single ASCII File Type character, a two binary byte Total Records per file number, a two byte spare location for future expansion and a two binary byte Program Start Address. This EOF Mark, like the Record Header information, is recorded as 16 true/complement data pairs totalling 32 bytes of information which facilitates error detection. EOF Mark ASCII characters are recorded with zero parity while the EOF Mark binary numbers use all eight bits to represent binary numbers.

File Mark Identifier — Single ASCII Character F
File Mark Identifier defines recorded information as EOF Mark.
File Name — Up to Eight ASCII Characters
Identical to record File Name
File Type — Single ASCII Character
Identical to record File Type
Total Records — Two Binary Bytes (0-FFFFH)
Total Records defines the total number of records in the file.
Spare — Two Bytes For Future Expressions

FIG. 2, FILE MARK FORMAT



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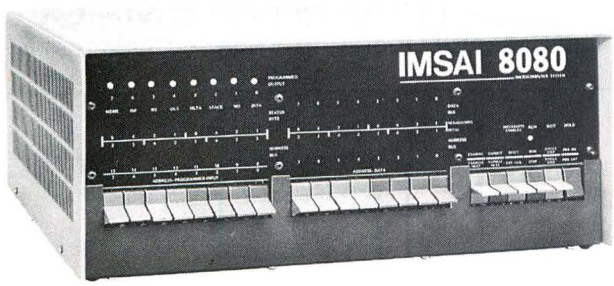

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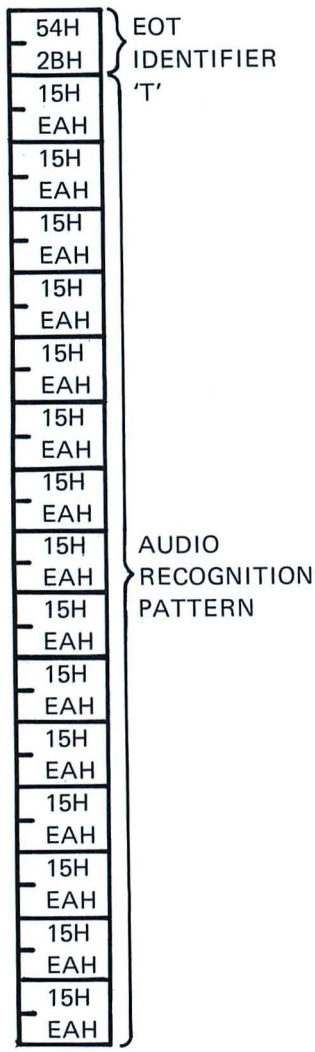
FIG. 3, TAPE MARK FORMAT



Program Start Address — Two Binary Bytes (0-FFFFH) Program Start Address defines RAM memory starting location for executable files.

END OF TAPE (EOT) MARK

EOT Mark identifies the end of tape and is recorded only after the GAP TO TAPE guard band following the last EOF Mark. EOT Mark information consists of a single ASCII character End Of Tape Identifier and an audible identification pattern of 30 bytes.

Tape Mark Identifier — Single ASCII Character T
Tape Mark Identifier defines recorded information as EOT Mark. EOT Identifier character recorded as a single true/complement data pair.
Audible Identification Pattern—Thirty Bytes
Audible Identification Pattern consists of 15H EAH 15H EAH 15H EAH . . . repeated for easy audible identification of EOT.

INTER RECORD GAP (IRG)

IRG consists of a minimum of 128 bytes of all ones or all zeroes, based on 200 bytes per second rate or equivalent time at other data rates.

GAP TO EOT MARK (GEOT)

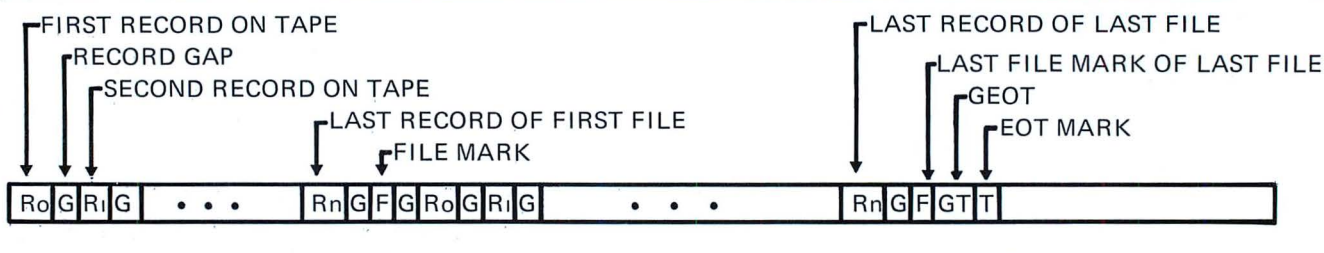
GEOT consists of a minimum of 256 bytes of all ones or all zeros, based on 200 bytes per second data rate or equivalent time at other data rates following EOF Mark of the last file on the tape.

TYPICAL RECORDED TAPE FORMAT

A typical recorded tape format is shown in figure 4, Cassette Tape Recording Format.

SECTION II - CASSETTE OPERATING SYSTEM - COS

The Cassette Operating System, COS, consists



NOTE: A single file mark is associated with each file and follows the last record of that file.

FIGURE 4, CASSETTE TAPE RECORDING FORMAT

of four commands - DATA SAVE, DATA LOAD, DATA VERIFY, and END OF TAPE commands. All numeric parameter entries are in HEX and may be from one to four HEX digits. Space delineates the hexadecimal parameters in the commands.

DATA SAVE COMMAND - CSAV

Saves contiguous memory locations and defines a file.

COMMAND SYNTAX:

CSAV "FILE NAME", TYPE (FIRST LOC) (LAST LOC) (RECORD LENGTH)

Record Length is an optional command input. File name, comma, and file type must be enclosed in double quotes. Spaces are not allowed between the comma and file type.

CSAV PARAMETER DEFINITIONS

File Name: Up to eight printable ASCII characters, exclusive of the comma, defined by the user. Leading, trailing, or imbedded spaces are not permitted.

Comma: Delineator between file name and file type.

Type: The file type specifies the data load start address source. If the file is a memory image file (I type), the file load start address is specified by FIRST LOC parameter, and the load start for each record is written on the tape header. If the file is any other type (R, A, B, or F), the load start is not specified in the record header on the tape.

First Loc: Specifies the first memory location to be saved on tape. First memory address location range is 0-FFFFH.

Last Loc: Specifies the last memory location to be stored on tape. Last memory address location range is 0-FFFFH.

Record Length (optional): The 256 byte (or 100H) record length will be used if the option is not invoked. The optional record length may be any reasonable value up to 64K (or FFFFH). Unless the file length is an integral number of record lengths, the last record will be short.

SAVE COMMAND EXAMPLES

Example 1: CSAV "ONE,I" 1000 1FFF

Defines a memory image file (I type) named ONE, starting at memory location 1000H and continuing through memory location 1FFFH and is recorded using the 256 (100H) byte record length. There would therefore be 16 (or 10H) full data records written on the tape.

Example 2: CSAV "TWO,R" 1000 1FFF 1000

Defines a relocatable memory image file (R type) named TWO, starting at memory location 1000H and continuing through 1FFFH and is recorded as one record 1000H bytes in length.

DATA LOAD COMMAND - CLOA

Loads contiguous memory locations as defined by the tape header or command. After the file is loaded, the file name contained in the tape header is printed.

COMMAND SYNTAX:

CLOA(S) "FILE NAME" (START OR BIAS) (FIRST RECORD #) (LAST RECORD #)

S, Start or Bias, First Record, and Last Record are optional command inputs.

CLOA PARAMETER DEFINITIONS

S (optional): After loading RAM memory with no errors, begin program execution at the location specified in the File Mark.

File Name (optional): If specified, the tape files will be searched for the file named within the double quotes. Leading, trailing, or imbedded spaces are not permitted. The file name must be enclosed in double quotes.

If not specified, the first complete file, based on the other input command parameters, will be loaded.

Start or Bias (optional): Specifies offset address bias.

If the type of file being loaded is a memory image (I), then this parameter is interpreted as a bias. Each record start load address is biased, effectively biasing the entire file to a new location. The total start plus bias may wrap around effectively giving a negative bias. Offset bias range is 0-FFFFH.

If the file is not a memory image (I) type, then this parameter is interpreted as a start load address for the file, and each succeeding record is loaded immediately following the last. Load address range if 0-FFFFH.

First Record # (optional): Specifies record number to be loaded into RAM memory.

If this parameter alone is specified, then only the one record number specified is loaded. Range of First Record Number is 0-FFFFH.

If this parameter is not specified, all records, starting with record zero of the file, are loaded.

Last Record # (optional): If this parameter is specified, contiguous records from the optional first record number through the optional last record number are loaded. Last Record number range is 0-FFFFH.

LOAD COMMAND EXAMPLES

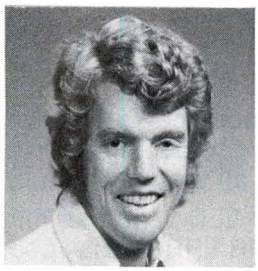
Example 1: CLOAS

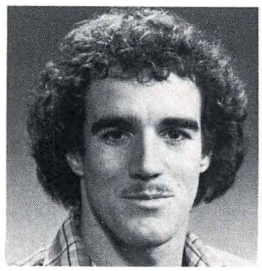
Loads the first complete file starting with record zero at the location specified on the tape header. File being loaded must be an I type. The optional 'S', when present, initiates execution of the program just loaded, assuming no errors, at the Program start address contained in the File Mark.

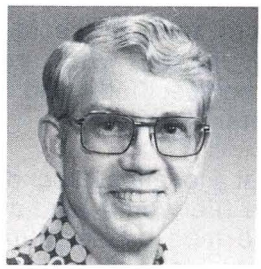
Example 2: CLOA "GAME1" FFFF

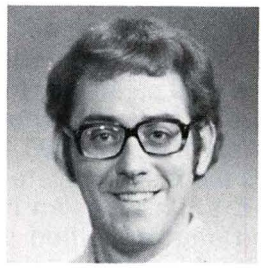
Searches the tape for record zero of the file named GAME and loads the file starting at the load

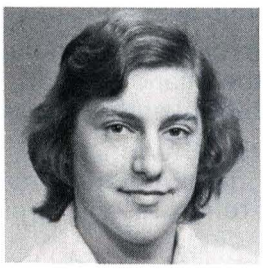
WE'RE PUTTING ALL OUR EGGHEADS IN ONE BASKET

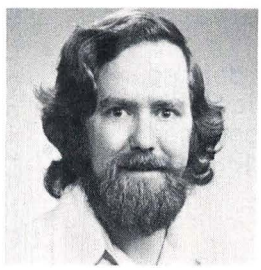

Michael Eusey

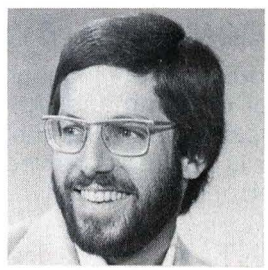

Paul Tripe


John Trotter


Jim Modecki


Steve Zook


Richard Henninger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start specified in the tape header minus one, assuming an I type file.

Example 3: CLOA "XYZ" 0 0

Searches the tape for record zero of the file named XYZ and loads only record zero with zero bias. The bias parameter must be specified to hold the place for the record number parameters.

Example 4: CLOA 1000

Loads the first complete file at a location depending on the file type. An I type file would load at the load start specified in the tape header plus 1000H. All files other than 1 type are loaded starting at location 1000H.

DATA VERIFY COMMAND - CVER

Verifies contiguous memory locations as defined by the tape header or command. After the file is successfully compared, the file name contained in the tape header is printed. The verify routine is aborted when an error is found.

COMMAND SYNTAX:

CVER "FILE NAME" (START OR BIAS) (FIRST RECORD #) (LAST RECORD #)
File Name, Start or Bias, First Record #, and Last Record # are optional command inputs.

CVER PARAMETER DEFINITIONS

The definition for all parameters is identical to the CLOA commands with the exception that the file is not loaded into memory but is compared with memory.

END OF TAPE COMMAND - MEOT

Marks end of tape.

COMMAND SYNTAX:

MEOT

COS RELATED ERROR MESSAGES

- **WHAT?**—Command syntax not correct.
- **NOT DIRECT LOAD TYPE**—File being loaded is not an I type and requires a start load address.
- **CRC ERROR**—Cyclic redundant check of data bytes and CRC on tape do not agree.
- **CASSETTE TIMEOUT**—Cassette interface output did not respond.
- **HEADER ERROR**—True complement byte pairs in the tape header are not correct.
- **RECORD NUMBER??**—The file being loaded contains non-contiguous record numbers.
- **EOT**—End of all files on tape has been reached.
- **NAME/TYPE?**—File name too long and/or file type not specified or delineated by a comma and/or type not acceptable.
- **VERIFIED**—File being verified is correct.
- **VERIFY ERROR XXXX YY ZZ**—Where XXXX is memory location, YY is tape data, and ZZ is memory data.

COS USER HINTS

- Allow enough room between files to allow the cassette drive to come to speed. Usually a few seconds is all that is required.
- Do not start a CLOA in the *middle* of a record. A HEADER ERROR may occur.
- Always use the MEOT command to mark the end of the tape so the system will not continue searching past the last file.
- Leave room between the last file and the end of tape mark to start the tape and write new files over the tape mark.
- Before CSAVing a file, record the cassette drive tape counter reading to allow fast forwarding to the area of the file when CLOAding.

COS FLOW DIAGRAMS

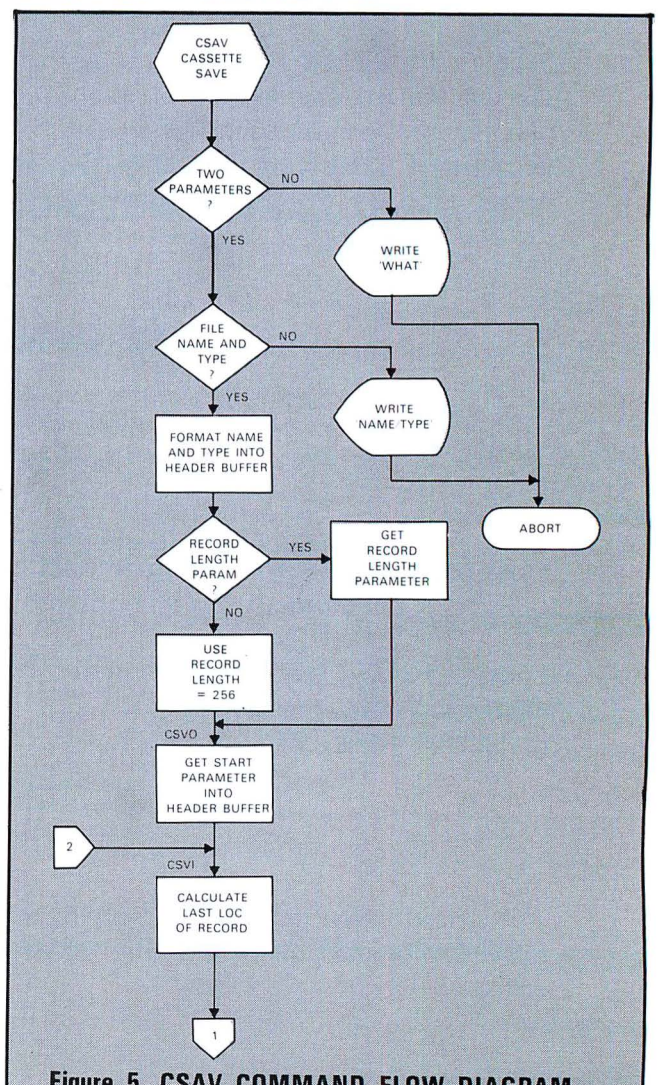

Figure 5. CSAV COMMAND FLOW DIAGRAM

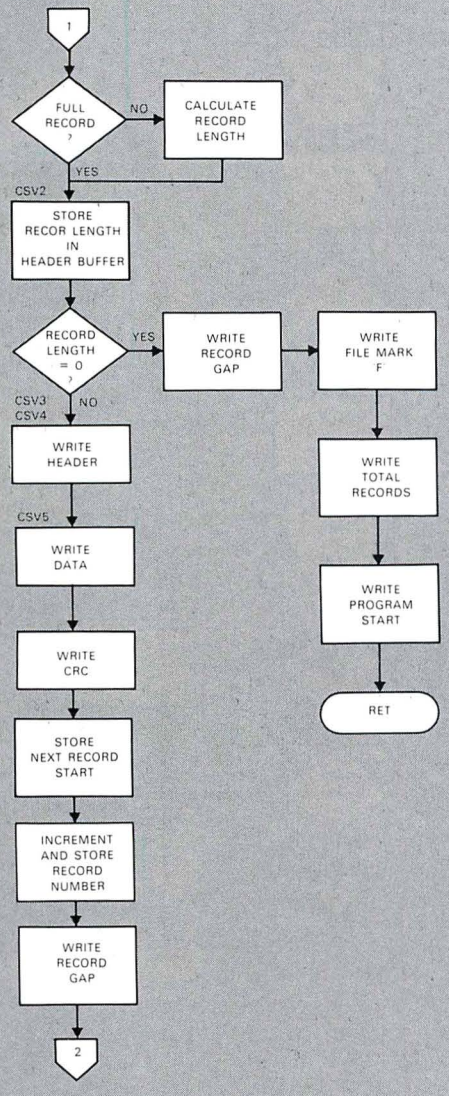

Figure 6. CSAV COMMAND FLOW DIAGRAM

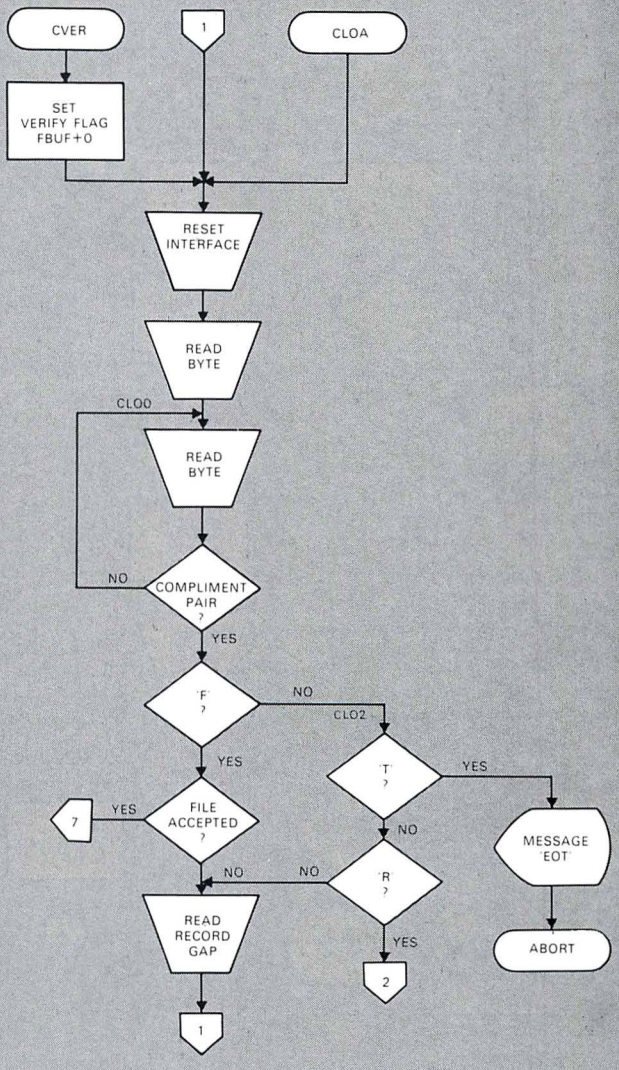

Figure 7. CVER COMMAND & CLOA COMMAND FLOW DIAGRAM

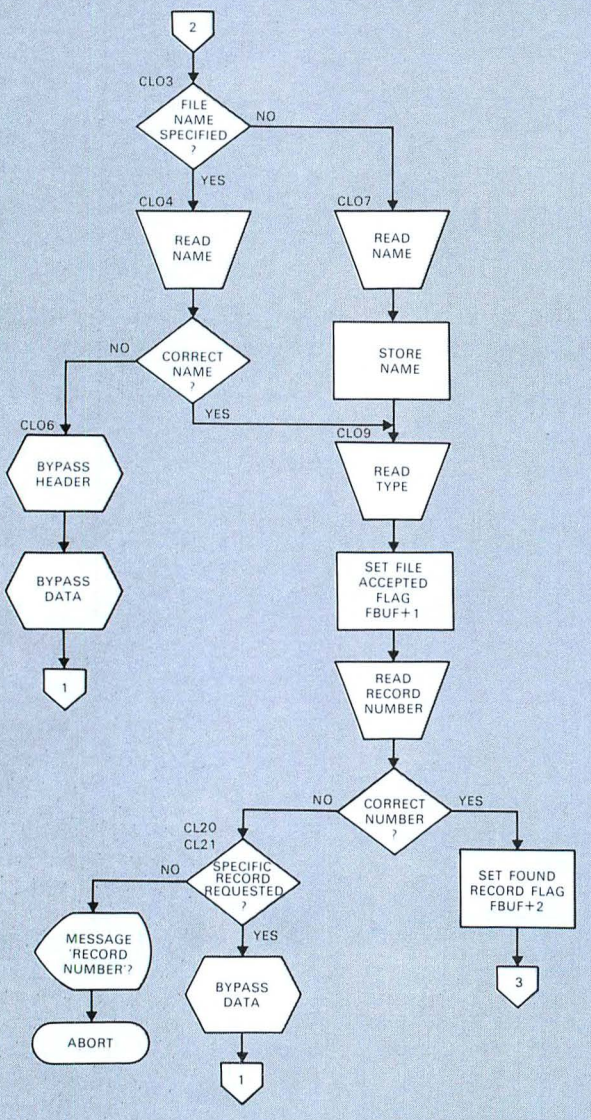

Figure 8. CVER COMMAND & CLOA COMMAND FLOW DIAGRAM — CONT. 1

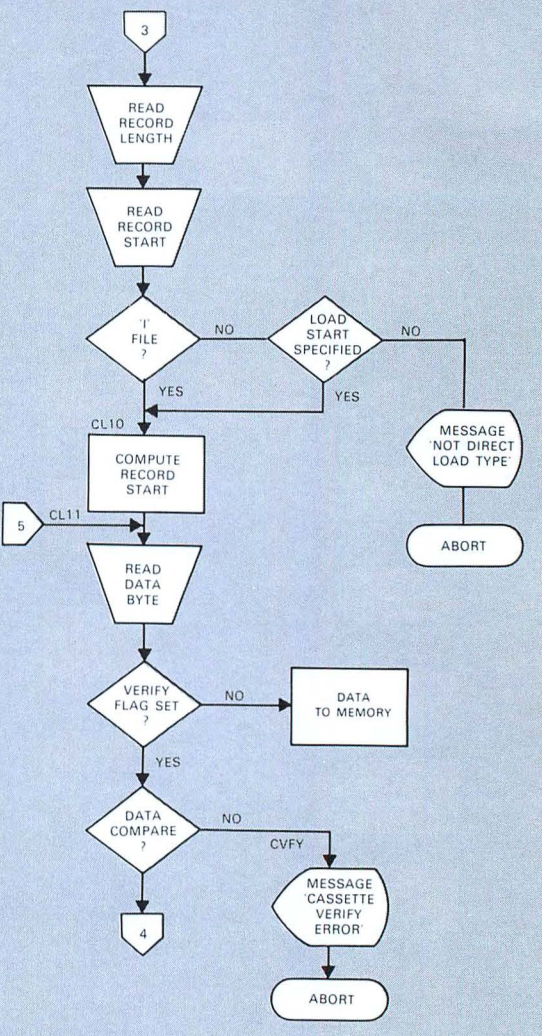

Figure 9. CVER COMMAND & CLOA COMMAND FLOW DIAGRAM — CONT. 2

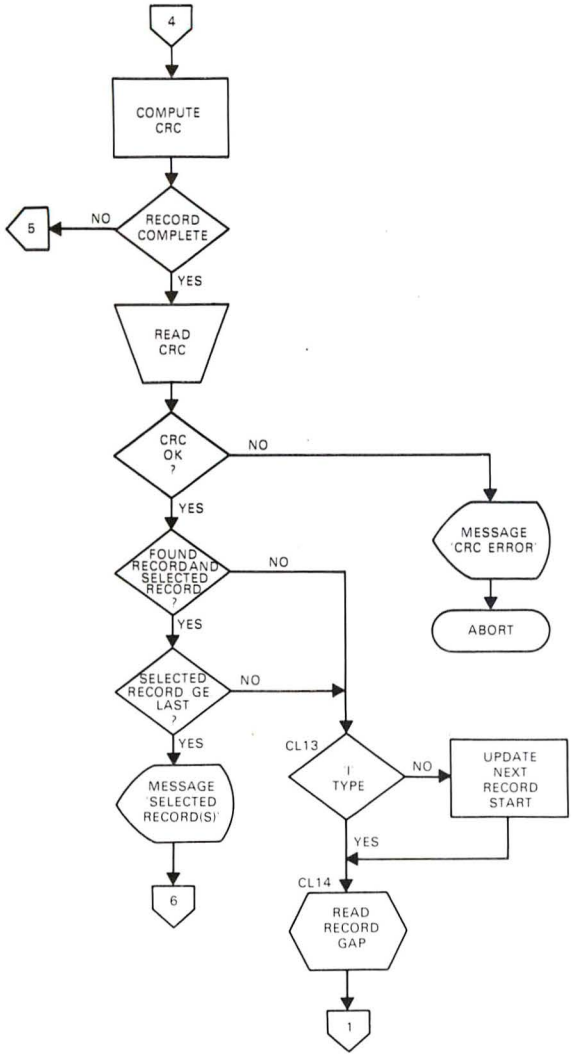

Figure 10. CVER COMMAND & CLOA COMMAND FLOW DIAGRAM CONT. 3

```
---
0000                    4070 *CASSETTTE OPERATING SYSTEM SUBROUTINES     <<< 503 LINES >>>
0000                    4075 *
0000                    4080 *ORIGIN: AUGUST 20,1976
0000                    4085 *REVISED: FEBRUARY 8,1977
0000                    4090 *PROGRAMMED BY: LORIN S. MOHLER
0000                    4095 *
0000                    4100 * BUFFER INITIALIZATION AND DEFINITION
0000                    4105 * ALL BUFFERS ARE INITIALIZED TO ZERO
0000                    4110 * ------------------------------------------------------
0000                    4115 * ASCII BUFFER: HOLD ASCII HEX PARAMETERS AS INPUT:
0000                    4120 * -                LEFT JUSTIFIED: FOUR DIGITS MAXIMUM
0000                    4125 * ABUF    - FIRST PARAMETER
0000                    4130 * ABUF+4  - SECOND PARAMETER
0000                    4135 * ABUF+8  - THIRD PARAMETER
0000                    4140 *
0000                    4145 * BINARY BUFFER: HOLD CONVERTED PARAMETERS: 16 BITS
0000                    4150 * BBUF    - FIRST PARAMETER
0000                    4155 * BBUF+2  - SECOND PARAMETER
0000                    4160 * BBUF+4  - THIRD PARAMETER
0000                    4165 *
0000                    4170 * TEXT BUFFER: HOLDS ASCII FILE NAME, COMMA DELINEATOR, AND TYPE
0000                    4175 * -               LEFT JUSTIFIED: TEN CHARACTERS MAXIMUM
0000                    4180 * TBUF    - FILE NAME, DELINEATOR, AND TYPE
0000                    4185 * ------------------------------------------------------
0000                    4190 *
0000                    4195 * SUBROUTINES CALLED BY THE CASSETTE ROUTINES
0000                    4200 * ------------------------------------------------------
0000                    4205 * PCK2 - A CALL TO THIS SUUBROUTINE WILL ABORT THE CALLING
0000                    4210 *                ROUTINE IF THE PARAMETERS ONE AND TWO HAVE NOT
0000                    4215 *                BEEN ENTERED.  CHECK FOR NON-NULL IN ABUF AND
0000                    4220 *                ABUF+4.
0000                    4225 *
0000                    4230 * ESCP - A CALL TO THIS SUBROUTINE WILL CHECK
0000                    4235 *                IF THE 'ESC' KEY HAS BEEN STRUCK, INDICATING THE
0000                    4240 *                OPERATOR WISHES TO ABORT THE PRESENT PROGRAM.
0000                    4245 *
0000                    4250 * CRLF - A CALL TO THIS SUBROUTINE WILL OUTPUT A CARRAIGE
0000                    4255 *                RETURN, LINE FEED, AND TWO SUBOUTS TO THE TELETYPE
0000                    4260 *
0000                    4265 * STRO - A CALL TO THIS SUBROUTINE WILL OUTPUT AN ASCII
0000                    4270 *                STRING POINTED TO BY HL REGISTERS AND WILL RETURN
0000                    4275 *                WHEN A CARRAIGE RETURN IS ENCOUNTERED IN THE STRING.
0000                    4280 * ------------------------------------------------------
0000                    4285 *
0000                    4290 *
0000                    4295 *
0000                    4300 *
0000                    4305 *  ----------------------
---
0000                    4310 *  CASSETTE SAVE ROUTINE
0000                    4315 *  CSAV / 'FILE NAME ,TYPE ' / FIRST LOC / LAST LOC / OPTIONAL REC LN
0000                    4320 *  ----------------------
0000 CD B6 05           4325 CSAV   CALL    PCK2        ;NEED FIRST AND LAST LOC
0003 CD 9F 08           4330        CALL    NTFT        ;FORMAT NAME AND TYPE INTO HEADER BUFFER
0006 2A 28 0F           4335        LHLD    BBUF        ;GET LOAD START
0009 22 30 0F           4340        SHLD    DBUF        ;STORE FOR AUTO START
000C 3A 1A 0F           4345        LDA     ABUF+8      ;SEE IF RECORD LN SPECIFIED
000F B7                 4350        ORA     A           ;SET COND
0010 2A 24 0F           4355        LHLD    BBUF+4      ;GET DATA REC LN
0013 C2 1C 00           4360        JNZ     CSV0        ;USE OPTIONAL DATA REC LN
0016 21 00 01           4365        LXI     H,100H      ;USE DATA REC LN OF 256 BYTES
0019 22 24 0F           4370        SHLD    BBUF+4      ;STORE RECORD LN
001C 2A 28 0F           4375 CSV0   LHLD    BBUF        ;GET START OF THIS RECORD
001F 3A 48 0F           4380        LDA     TBUF+8      ;CHECK FILE TYPE
0022 FE 49              4385        CPI     'I'         ;IMAGE FILE ?
0024 C2 2A 00           4390        JNZ     CSV1        ;YES.  REC START TO HEADER BUFFER
0027 22 4D 0F           4395        SHLD    TBUF+13     ;
002A EB                 4400 CSV1   XCHG                ;REC START TO <DE>
002B 2A 24 0F           4405        LHLD    BBUF+4      ;GET REC LN
002E 19                 4410        DAD     D           ;MAKE LAST LOC OF REC+1
002F 2B                 4415        DCX     H           ;MOVE THE LAST LOC
0030 EB                 4420        XCHG                ;PUT IN <DE>
0031 2A 22 0F           4425        LHLD    BBUF+2      ;GET END OF FILE
0034 7D                 4430        MOV     A,L         ;SEE IF REC PAST END OF FILE
0035 93                 4435        SUB     E           ;
0036 5F                 4440        MOV     E,A         ;
0037 7C                 4445        MOV     A,H         ;
0038 9A                 4450        SBB     D           ;<DE> HAS NO. BYTES 'TILL EOF
0039 57                 4455        MOV     D,A         ;IF NEG THEN NO. PAST END
003A 2A 24 0F           4460        LHLD    BBUF+4      ;GET REC LN
003D D2 41 00           4465        JNC     CSV2        ;FULL LN REC
0040 19                 4470        DAD     D           ;SHORT LAST REC
0041 22 4B 0F           4475 CSV2   SHLD    TBUF+11     ;STORE LN OF THIS REC
0044 7D                 4480        MOV     A,L         ;REC LN EQUAL ZERO ?
0045 B4                 4485        ORA     H           ;
0046 C2 50 00           4490        JNZ     CSV3        ;NO.  OUTPUT MORE RECORDS
0049 CD E6 00           4495        CALL    WRGP        ;NEED A GAP
004C CD F1 00           4500        CALL    MEOF        ;YES.  END OF FILE.  MARK IT
004F C9                 4505        RET                 ;THAT'S ALL
0050 3E 3C              4510 CSV3   MVI     A,3CH       ;START BYTE
0052 CD 33 00           4515        CALL    CSOH        ;CASSETTE OUTPUT
0055 3E E6              4520        MVI     A,0E6H      ;SYNC BYTE
0057 CD 33 00           4525        CALL    CSOH        ;
005A 3E 52              4530        MVI     A,'R'       ;RECORD ID
005C CD 2B 00           4535        CALL    CSOP        ;CASSETTE OUTPUT ( TRUE/COMP )
005F 11 40 0F           4540        LXI     D,TBUF      ;POINT TO HEADER DATA
0062 0E 0F              4545        MVI     C,15        ;BYTES TO PROCESS
---
0064 1A                 4550 CSV4   LDAX    D           ;GET HEADER DATA
0065 CD 2B 00           4555        CALL    CSOP        ;CASSETTE OUTPUT ( TRUE/COMP )
0068 13                 4560        INX     D           ;
0069 0D                 4565        DCR     C           ;
006A C2 64 00           4570        JNZ     CSV4        ;THE WHOLE THING
006D 2A 4B 0F           4575        LHLD    TBUF+11     ;GET REC LN
0070 EB                 4580        XCHG                ;PUT IN <DE>
0071 2A 20 0F           4585        LHLD    BBUF        ;START LOAD ADDRESS
0074 01 FF FF           4590        LXI     B,0FFFFH    ;INITIALIZE CRC
0077 D5                 4595 CSV5   PUSH    D           ;SAVE REC LN COUNT
0078 7E                 4600        MOV     A,M         ;GET M DATA BYTE
0079 CD 33 00           4605        CALL    CSOH        ;CASSETTE OUTPUT
007C CD 67 00           4610        CALL    CRCX        ;CRC ROUTINE
007F 23                 4615        INX     H           ;POINT TO NEXT LOC
0080 D1                 4620        POP     D           ;GET REC LN COUNT
0081 1B                 4625        DCX     D           ;DCR REC LN
0082 7B                 4630        MOV     A,E         ;SEE IF DONE
0083 B2                 4635        ORA     D           ;
0084 C2 77 00           4640        JNZ     CSV5        ;ANY BYTES LEFT IN RECORD ?
0087 79                 4645        MOV     A,C         ;NO.  WRITE CRC
0088 CD 2B 00           4650        CALL    CSOP        ;CASSETTE OUTPUT ( TRUE/COMP )
008B 78                 4655        MOV     A,B         ;WRITE REST OF CRC
008C CD 2B 00           4660        CALL    CSOP        ;CASSETTE OUTPUT ( TRUE/COMP )
008F 22 20 0F           4665        SHLD    BBUF        ;REC START FOR NEXT RECORD
0092 2A 49 0F           4670        LHLD    TBUF+9      ;GET REC NUMBER.  FIRST =0
0095 23                 4675        INX     H           ;INCREMENT IT
0096 22 49 0F           4680        SHLD    TBUF+9      ;PUT IT BACK
0099 CD E6 00           4685        CALL    WRGP        ;WRITE A RECORD GAP
009C C3 1C 00           4690        JMP     CSV0        ;GO WRITE MORE RECORDS
009F                    4695 *  ----------------------
009F                    4700 *  FILE NAME AND TYPE FORMAT INTO HEADER BUFFER
009F                    4705 *  ----------------------
009F 21 3F 0F           4710 NTFT   LXI     H,TBUF-1    ;POINT TO BUFFER AREA
```

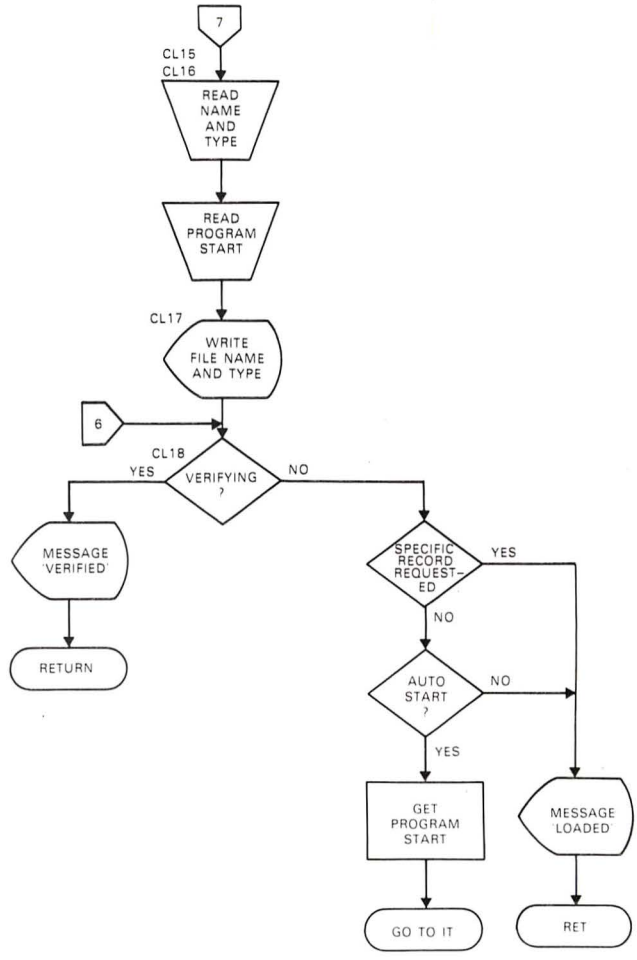

Figure 11. CVER COMMAND & CLOA COMMAND FLOW DIAGRAM — CONT. 4

```
08A2 0E 0A          4715          MVI     C,10        ;FILE NAME + TYPE LENGTH
08A4 0D             4720 NTF1     DCR     C           ;COUNT POSITION
08A5 CA CE 08       4725          JZ      NTF3        ;NO TYPE
08A8 23             4730          INX     H           ;NEXT POSITION
08A9 7E             4735          MOV     A,M         ;GET A CHARACTER
08AA FE 2C          4740          CPI     ','         ;TYPE DELINEATOR ?
08AC C2 A4 08       4745          JNZ     NTF1        ;NO. KEEP LOOKING
08AF 36 00          4750          MVI     M,0         ;YES. SO NULL IT OUT
08B1 23             4755          INX     H           ;NEXT IS TYPE
08B2 7E             4760          MOV     A,M         ;SAVE TYPE
08B3 FE 41          4765          CPI     'A'         ;IS TYPE
08B5 DA CE 08       4770          JC      NTF3        ; 'A' THROUGH 'Z' ?
08B8 FE 5B          4775          CPI     'Z'+1       ;BETTER BE
08BA D2 CE 08       4780          JNC     NTF3        ;
08BD 36 00          4785 NTF2     MVI     M,0         ;NULL CHARACTER IN TBUF
---
08BF 23             4790          INX     H           ;NULL REST OF NAME AREA
08C0 0D             4795          DCR     C           ;KEEP TRACK
08C1 C2 BD 08       4800          JNZ     NTF2        ;ALL OF IT
08C4 32 40 0F       4805          STA     TBUF+8      ;PUT TYPE AT TBUF+8
08C7 21 00 00       4810          LXI     H,0         ;MAKE A BIG ZERO
08CA 22 49 0F       4815          SHLD    TBUF+9      ;ZERO THE RECORD NUMBER
08CD C9             4820          RET                 ;DONE
08CE CD 0A 06       4825 NTF3     CALL    CRLF        ;NEATNESS
08D1 21 DA 08       4830          LXI     H,NTYM      ;POINT TO MESSAGE
08D4 CD 52 01       4835          CALL    STRO        ;WRITE IT OUT
08D7 C3 56 00       4840          JMP     ABRT        ;ABORT
08DA 4E 41 4D 45    4845 NTYM     ASC     'NAME/TYPE ?'
     2F 54 59 50
     45 20 3F
08E5 0D             4850          DB      13
08E6                4855 *  ======================
08E6                4860 *  WRITE RECORD GAP
08E6                4865 *  ======================
08E6 06 80          4870 WRGP     MVI     B,80H       ;GAP BYTES
08E8 AF             4875          XRA     A           ;ZEROS
08E9 CD 33 09       4880 WRG1     CALL    CSOH        ;CASSETTE OUTPUT
08EC 05             4885          DCR     B           ;BYTE COUNT
08ED C2 E9 08       4890          JNZ     WRG1        ;MORE ?
08F0 C9             4895          RET                 ;NONE
08F1                4900 *  ======================
08F1                4905 *  WRITE FILE MARK FOR END OF FILE
08F1                4910 *  ======================
08F1 3E 3C          4915 MEOF     MVI     A,3CH       ;MAKE START BYTE
08F3 CD 33 09       4920          CALL    CSOH        ;CASSETTE OUTPUT
08F6 3E E6          4925          MVI     A,0E6H      ;MAKE A STAC BYTE
08F8 CD 33 09       4930          CALL    CSOH        ;
08FB 3E 46          4935          MVI     A,'F'       ;FILE MARK ID - EOF
08FD CD 2B 09       4940          CALL    CSOF        ;CASSETTE OUTPUT ( TRUE/COMP )
0900 0E 09          4945          MVI     C,9         ;HEADER BYTE COUNT
0902 11 4D 0F       4950 MEF1     LXI     D,TBUF      ;POINT TO HEADER DATA
0905 CD 2B 09       4955          CALL    CSOF        ;CASSETTE OUTPUT
0908 0D             4960          DCR     C           ;LESS TO DO
0909 C2 02 09       4965          JNZ     MEF1        ;
090C 2A 49 0F       4970          LHLD    TBUF+9      ;NOW HAS TOTAL RECORDS
090F 7D             4975          MOV     A,L         ;
0910 CD 2B 09       4980          CALL    CSOF        ;
0913 7C             4985          MOV     A,H         ;
0914 CD 2B 09       4990          CALL    CSOF        ;WRITE TOTAL RECORDS
0917 AF             4995          XRA     A           ;
0918 CD 2B 09       5000          CALL    CSOF        ;
091B AF             5005          XRA     A           ;
091C CD 2B 09       5010          CALL    CSOF        ;WRITE NULL SPARE
091F 2A 30 0F       5015          LHLD    DBUF        ;GET START FOR AUTO START
---
0922 7D             5020          MOV     A,L         ;WRITE PROG START ( LO )
0923 CD 2B 09       5025          CALL    CSOF        ;
0926 7C             5030          MOV     A,H         ;WRITE PROG START ( HI )
0927 CD 2B 09       5035          CALL    CSOF        ;
092A C9             5040          RET                 ;DONE
092B                5045 *  ======================
092B                5050 *  WRITE CASSETTE DATA TRUE / COMPLIMENT PAIR
092B                5055 *  ======================
092B CD 33 09       5060 CSOF     CALL    CSOH        ;WRITE TRUE DATA
092E 2F             5065          CMA                 ;COMPLIMENT THE DATA
092F CD 33 09       5070          CALL    CSOH        ;WRITE COMPLIMENT
0932 C9             5075          RET                 ;BYE
0933                5080 *  ======================
0933                5085 *  CASSETTE OUTPUT HANDLER
0933                5090 *  ======================
0933 D5             5095 CSOH     PUSH    D           ;SAVE <DE>
0934 F5             5100          PUSH    PSW         ;SAVE DATA + FLAGS
0935 11 00 00       5105          LXI     D,0         ;INITIALIZE TIMER
0938 13             5110 CSO1     INX     D           ;SEQUENCE TIMER
0939 CD 1D 06       5115          CALL    ESCP        ;WANT OUT ?
093C 7A             5120          MOV     A,D         ;CHECK TIMER
093D B7             5125          ORA     A           ;SET CONDS
093E FA 27 0C       5130          JM      CSTO        ;DEVICE TIMEOUT ERROR
0941 DB 6E          5135          IN      CASC        ;CASSETTE STATUS
0943 E6 20          5140          ANI     20H         ;READY BIT
0945 C2 38 09       5145          JNZ     CSO1        ;READY IF ZERO
0948 F1             5150          POP     PSW         ;GET DATA
0949 D3 6F          5155          OUT     CASD        ;CASSETTE OUTPUT PORT
094B D1             5160          POP     D           ;RESTORE <DE>
094C C9             5165          RET                 ;ONE BYTE OUTPUT, WHEW
094D                5170 *  ======================
094D                5175 *  CASSETTE VERIFY ROUTINE
094D                5180 *  CVER / *OPT FILE NAME* / OPT BIAS / OPT REC NO. / OPT LAST REC NO. /
094D                5185 *  CVER / FIRST VERIFY LOC FOR NON "I" TYPE /
094D                5190 *  ======================
094D 3E FF          5195 CVER     MVI     A,0FFH      ;MAKE VERIFY ONLY FLAG
094F 32 39 0F       5200          STA     FBUF        ;FLAG9
0952                5205 *  ======================
0952                5210 *  CASSETTE INPUT ROUTINE
0952                5215 *  CLOA(S) / *OPT FILE NAME* / OPT BIAS / OPT REC NO. / OPT LAST REC NO. /
0952                5220 *  CLOA(S) / FIRST LOAD LOC FOR NON "I" TYPE /
0952                5225 *  ======================
0952 3E 10          5230 CLOA     MVI     A,10H       ;MAKE AN INTERFACE RESET
0954 D3 6E          5235          OUT     CASC        ;DO IT
0956 CD 01 0C       5240          CALL    CSIH        ;READ TRUE
0959 47             5245          MOV     B,A         ;SAVE DATA
095A CD 01 0C       5250 CLO0     CALL    CSIH        ;READ COMPLIMENT
095D 2F             5255          CMA                 ;COMPLIMENT
---
095E B8             5260          CMP     B           ;A PAIR ?
095F CA 67 09       5265          JZ      CLO1        ;YES
0962 2F             5270          CMA                 ;NO. RESTORE
0963 47             5275          MOV     B,A         ;SAVE BYTE
0964 C3 5A 09       5280          JMP     CLO0        ;TRY AGAIN
0967 FE 46          5285 CLO1     CPI     'F'         ;FILE MARK ?
0969 C2 79 09       5290          JNZ     CLO2        ;NO. CONTINUE
096C 3A 39 0F       5295          LDA     FBUF+1      ;YES. GET FILE ACCEPTED FLAG
096F B7             5300          ORA     A           ;HAS SEARCHED FOR FILE BEEN ACCEPTED ?
0970 C2 95 0A       5305          JNZ     CL15        ;YES. GO CLEAN UP
0973 CD AA 0B       5310          CALL    RBGP        ;NO. READ A REC GAP
0976 C3 52 09       5315          JMP     CLOA        ;SEARCH FOR CORRECT FILE
0979 FE 54          5320 CLO2     CPI     'T'         ;TAPE MARK ?
097B CA C9 0B       5325          JZ      CEOT        ;YES. EOT
097E FE 52          5330          CPI     'R'         ;RECORD MARK ?
0980 CA 89 09       5335          JZ      CLO3        ;YES. HAVE AT IT
0983 CD AA 0B       5340          CALL    RBGP        ;NO. READ THE GAP
0986 C3 52 09       5345          JMP     CLOA        ;AND CONTINUE
0989 3A 40 0F       5350 CLO3     LDA     TBUF        ;FOUND A RECORD
098C B7             5355          ORA     A           ;FILE NAME SPECIFIED ?
098D CA B7 09       5360          JZ      CLO7        ;NO.
0990 16 09          5365          MVI     D,9         ;YES. PROCESS
0992 21 3F 0F       5370          LXI     H,TBUF-1    ;POINT TO NAME
0995 23             5375 CLO4     INX     H           ;NEXT POSITION
0996 15             5380          DCR     D           ;POSITION COUNT
0997 CA C5 09       5385          JZ      CLO9        ;VERIFIED ALL ?
099A CD D9 0B       5390          CALL    CSIP        ;NO. READ COMPLIMENT PAIR
099D BE             5395          CMP     M           ;RIGHT FILE ?
099E CA 95 09       5400          JZ      CLO4        ;YES. OK SO FAR
09A1 15             5405 CLO5     DCR     D           ;NO. EAT THE REST
09A2 CA AB 09       5410          JZ      CLO6        ;THAT ALL ?
09A5 CD D9 0B       5415          CALL    CSIP        ;NOT YET
09A8 C3 A1 09       5420          JMP     CLO5        ;MORE
09AB CD D9 0B       5425 CLO6     CALL    CSIP        ;TYPE ENTER
09AE CD D9 0B       5430          CALL    CSIP        ;EAT A PAIR, REC NUMBER ( LOW )
09B1 CD D9 0B       5435          CALL    CSIP        ;AND ANOTHER, REC NUMBER ( HI )
09B4 C3 0F 0B       5440          JMP     BPDT        ;BYPASS THE REST OF RECORD
09B7 16 08          5445 CLO7     MVI     D,8         ;GET NAME
09B9 21 3F 0F       5450          LXI     H,TBUF-1    ;FROM TAPE AND SAVE IT
09BC 23             5455 CLO8     INX     H           ;
09BD CD D9 0B       5460          CALL    CSIP        ;READ A PAIR
09C0 77             5465          MOV     M,A         ;PUT IN TBUF
09C1 15             5470          DCR     D           ;COUNT
09C2 C2 BC 09       5475          JNZ     CLO8        ;DO MORE
09C5 CD D9 0B       5480 CLO9     CALL    CSIP        ;READ TYPE
09C8 32 48 0F       5485          STA     TBUF+8      ;STORE IN HEADER BUFFER
09CB 3E FF          5490          MVI     A,0FFH      ;MAKE FILE ACCEPTED FLAG
09CD 32 39 0F       5495          STA     FBUF+1      ;STORE IT
---
0900 2A 22 0F       5500          LHLD    BBUF+2      ;GET RECORD NUMBER
0903 CD D9 0B       5505          CALL    CSIP        ;READ REC NUMBER (LOW)
0906 BD             5510          CMP     L           ;OK ?
0907 C2 F8 0A       5515          JNZ     CL20        ;NO. BYPASS REC AND RETRY
090A CD D9 0B       5520          CALL    CSIP        ;YES. READ REC NUMBER (HI)
090D BC             5525          CMP     H           ;OK ?
090E C2 FB 0A       5530          JNZ     CL21        ;NO. BYPASS REC AND RETRY
0911 22 49 0F       5535          SHLD    TBUF+9      ;STORE THIS REC NO. IN BUFFER
0914 23             5540          INX     H           ;YES. CORRECT REC NUMBER
0915 22 22 0F       5545          SHLD    BBUF+2      ;SO. INCREMENT IT AND STORE IT FOR NEXT
0918 3E FF          5550          MVI     A,0FFH      ;FOUND REQUIRED RECORD
091A 32 3A 0F       5555          STA     FBUF+2      ;SET FLAG
091D 3E 07          5560          MVI     A,7         ;ACCEPTANCE 'BELL'
091F D3 01          5565          OUT     TTOP        ;DING-DONG
0921 CD D9 0B       5570          CALL    CSIP        ;READ REC LN (LOW)
0924 4F             5575          MOV     C,A         ;
0925 CD D9 0B       5580          CALL    CSIP        ;READ REC LN (HI)
0928 47             5585          MOV     B,A         ;PUT IN <BC>
0929 C5             5590          PUSH    B           ;SAVE REC LN COUNT
092A CD D9 0B       5595          CALL    CSIP        ;GET REC START (LO)
092D 5F             5600          MOV     E,A         ;
092E CD D9 0B       5605          CALL    CSIP        ;READ REC START (HI)
0931 57             5610          MOV     D,A         ;PUT IN <DE>
0932 3A 48 0F       5615          LDA     TBUF+8      ;GET FILE TYPE
0935 FE 49          5620          CPI     'I'         ;IMAGE FILE ?
0937 CA 14 0A       5625          JZ      CL10        ;YES
093A 11 00 00       5630          LXI     D,0         ;NO. FORCE LOAD REC START DATA = ZERO
093D 3A 12 0F       5635          LDA     ABUF        ;WAS LOAD START LOC SPECIFIED ?
0940 B7             5640          ORA     A           ;
0941 CA 1B 0B       5645          JZ      NDLF        ;INCOMPATIBLE - EXIT
0944 2A 20 0F       5650 CL10     LHLD    BBUF        ;GET FORCED REC START (NON I), OR BIAS (I)
0947 19             5655          DAD     D           ;MAKE A BIASED REC START OR FORCED REC START
0948 D1             5660          POP     D           ;REC LN COUNT TO <DE>
0949 01 FF FF       5665          LXI     B,0FFFFH    ;INITIALIZE CRC
094C C5             5670 CL11     PUSH    B           ;SAVE CRC
094D CD 01 0C       5675          CALL    CSIH        ;READ DATA BYTE
0950 4F             5680          MOV     C,A         ;SAVE DATA BYTE
0951 3A 38 0F       5685          LDA     FBUF        ;VERIFY ONLY ?
0954 B7             5690          ORA     A           ;CHECK FLAG9
0955 79             5695          MOV     A,C         ;DATA TO REG. A
0956 C2 2A 0A       5700          JNZ     CL12        ;FLAG SET, VERIFY ONLY
0959 77             5705          MOV     M,A         ;PUT DATA IN MEMORY
095A BE             5710 CL12     CMP     M           ;DOES IT VERIFY
095B C2 3C 0B       5715          JNZ     CVFY        ;CASSETTE VERIFY ERROR, ABORT
095E C1             5720          POP     B           ;RESTORE CRC
095F CD 67 0B       5725          CALL    CRCX        ;CRC ROUTINE
0962 23             5730          INX     H           ;NEXT MEM LOC
0963 1B             5735          DCX     D           ;DECR REC LN COUNT
---
0964 7B             5740          MOV     A,E         ;
0965 B2             5745          ORA     D           ;SEE IF ZERO
0966 C2 1C 0A       5750          JNZ     CL11        ;NO. READ MORE DATA
0969 22 30 0F       5755          SHLD    DBUF        ;SAVE NEXT REC START (NON I)
096C CD D9 0B       5760          CALL    CSIP        ;READ CRC. COMPAIR
096F B9             5765          CMP     C           ;CHECK ?
0970 C2 44 0C       5770          JNZ     CRCE        ;CRC ERROR
0973 CD D9 0B       5775          CALL    CSIP        ;READ CRC COMPAIR
0976 B8             5780          CMP     B           ;CHECK ?
0977 C2 44 0C       5785          JNZ     CRCE        ;NO. CRC ERROR
097A 21 3A 0F       5790          LXI     H,FBUF+2    ;POINT TO RECORD FOUND FLAG
097D 3A 16 0F       5795          LDA     ABUF+4      ;SPECIFIC RECORD REQUESTED ?
0980 A6             5800          ANA     M           ;BOTH THERE ?
0981 CA 81 0A       5805          JZ      CL13        ;NO. KEEP ON
0984 2A 24 0F       5810          LHLD    BBUF+4      ;GET LAST REC PARAM
0987 3A 49 0F       5815          LDA     TBUF+9      ;PRESENT REC NO. ( LO )
098A 95             5820          SUB     L           ;
098B 3A 4A 0F       5825          LDA     TBUF+10     ;PRESENT REC NO. ( HI )
098E 9C             5830          SBB     H           ;SEE IF PRESENT REC NO.
098F DA 81 0A       5835          JC      CL13        ;IS .GE. LAST REC PARAM
0992 CD 0A 06       5840          CALL    CRLF        ;PARTIAL FILE LOADING COMPLETE
0995 21 6E 0A       5845          LXI     H,SELM      ;POINT TO MESSAGE
0998 CD 52 01       5850          CALL    STRO        ;WRITE IT OUT
099B C3 C7 0A       5855          JMP     CL18        ;MORE TO THE MESSAGE
099E 53 45 4C 45    5860 SELM     ASC     'SELECTED RECORD(S)'
     43 54 45 44
     20 52 45 43
     4F 52 44 28
     53 29
09B0 0D             5865          DB      13
09B1 2A 30 0F       5870 CL13     LHLD    DBUF        ;UPDATE REC START (NON I)
09B4 3A 48 0F       5875          LDA     TBUF+8      ;GET TYPE
09B7 FE 49          5880          CPI     'I'         ;IS IT 'I' TYPE
09B9 CA 0F 0A       5885          JZ      CL14        ;YES. BBUF HAS BIAS. DON'T TOUCH
09BC 22 20 0F       5890          SHLD    BBUF        ;NO. NOW I. NEED CONTIGUOUS REC START
09BF CD AA 0B       5895 CL14     CALL    RBGP        ;RECORD GAP HERE
09C2 C3 52 09       5900          JMP     CLOA        ;AND CONTINUE
09C5 0E 0D          5905 CL15     MVI     C,13        ;GET PAST
09C7 CD D9 0B       5910 CL16     CALL    CSIP        ;NAME AND TYPE AND
09CA 0D             5915          DCR     C           ;NO. RECORDS AND SPARE
09CB C2 C7 0A       5920          JNZ     CL16        ;KEEP ON KEEPING ON
09CE CD D9 0B       5925          CALL    CSIP        ;GET PROG START ( LO )
09D1 6F             5930          MOV     L,A         ;
09D2 CD D9 0B       5935          CALL    CSIP        ;GET PROG START ( HI )
09D5 67             5940          MOV     H,A         ;INTO <HL>
09D6 22 32 0F       5945          SHLD    DBUF+2      ;SAVE PROG START
09D9 CD D5 06       5950          CALL    CRLF        ;DISPLAY WHAT'S HAPPENING
09DC 0E 08          5955          MVI     C,8         ;MAX LENGTH OF FILE NAME
---
09DE 21 40 0F       5960          LXI     H,TBUF      ;POINT TO FILE NAME
09E1 7E             5965 CL17     MOV     A,M         ;GET NAME
09E2 23             5970          INX     H           ;POINT TO NEXT
09E3 47             5975          MOV     B,A         ;OUTPUT TO VIDEO
09E4 CD 3E 06       5980          CALL    TTOH        ;DO IT
09E7 0D             5985          DCR     C           ;LESS NAME TO DO
09E8 C2 E1 0A       5990          JNZ     CL17        ;MORE NAME
09EB 06 2C          5995          MVI     B,','       ;FILE TYPE SEPERATOR
09ED CD 3E 06       6000          CALL    TTOH        ;WRITE IT
09F0 3A 48 0F       6005          LDA     TBUF+8      ;GET TYPE
09F3 47             6010          MOV     B,A         ;WRITE IT OUT
09F4 CD 3E 06       6015          CALL    TTOH        ;
09F7 CD D3 05       6020 CL18     CALL    SPC1        ;WRITE A SPACE
09FA 3A 38 0F       6025          LDA     FBUF        ;VERIFY ?
09FD B7             6030          ORA     A           ;'LOADED' OR 'VERIFIED'
09FE C2 25 05       6035          JNZ     VRFD        ;MESSAGE 'VERIFIED'
0A01 3A 16 0F       6040          LDA     ABUF+4      ;SPECIFIC RECORD SELECTED ?
0A04 B7             6045          ORA     A           ;
0A05 C2 E7 0A       6050          JNZ     CL19        ;YES. SORRY NO AUTO START
0A08 3A 94 0F       6055          LDA     IBUF+4      ;GET INPUT BUFFER 5TH CHAR
0A0B FE 53          6060          CPI     'S'         ;AUTO START ?
0A0D C2 E7 0A       6065          JNZ     CL19        ;NO. FINISH UP
0A10 CD D0 06       6070          CALL    CRLF        ;CERTAINLY
0A13 2A 32 0F       6075          LHLD    DBUF+2      ;YES. GET PROG START
0A16 E9             6080          PCHL                ;GO TO IT
0A17 21 F1 0A       6085 CL19     LXI     H,LODM      ;MESSAGE 'LOADED'
0A1A CD 52 01       6090          CALL    STRO        ;MESSAGE TO SCREEN
0A1D CD D0 06       6095          CALL    CRLF        ;NOW NOT ?
0A20 C9             6100          RET                 ;THAT'S ALL FOLKS
0A21 4C 4F 41 44    6105 LODM     ASC     'LOADED'
     45 44
0A27 0D             6110          DB      13          ;LOADED
0A28 CD D9 0B       6115 CL20     CALL    CSIP        ;GET PAST REC NUMBER (HI)
0A2B 3A 16 0F       6120 CL21     LDA     ABUF+4      ;WAS SPECIFIC RECORD REQUESTED ?
0A2E B7             6125          ORA     A           ;ANYTHING THERE
0A2F C2 07 0B       6130          JNZ     BPDT        ;YES. BYPASS AND TRY AGAIN
0A32 21 0B 0B       6135          LXI     H,RNEM      ;NO. THERFORE NOT CONTIGUOUS REC NUMB
0A35 CD 52 01       6140          CALL    STRO        ;WRITE ERROR MESSAGE
0A38 C3 56 00       6145          JMP     ABRT        ;ABORT
0A3B 52 45 43 4F    6150 RNEM     ASC     'RECORD NUMBER ?'
     52 44 20 4E
     55 4D 42 45
     52 20 3F
0A1A 0D             6155          DB      13
0A1B CD 0A 06       6160 NDLF     CALL    CRLF        ;NEAT AGAIN
0A1E 21 27 0B       6165          LXI     H,NDLM      ;POINT TO MESSAGE
0A21 CD 52 01       6170          CALL    STRO        ;WRITE IT OUT
0A24 C3 56 00       6175          JMP     ABRT        ;EXIT
---
0A27 4E 4F 54 20    6180 NDLM     ASC     'NOT DIRECT LOAD TYPE'
     44 49 52 45
     43 54 20 4C
     4F 41 44 20
     54 59 50 45
0A38 0D             6185          DB      13
0A3C                6190 *  ======================
0A3C                6195 *  CASSETTE VERIFY ERROR
0A3C                6200 *  ======================
0A3C 32 35 0F       6205 CVFY     STA     DBUF+5      ;SAVE TAPE DATA
0A3F 7E             6210          MOV     A,M         ;GET MEMORY DATA
0A40 32 36 0F       6215          STA     DBUF+6      ;SAVE MEMORY DATA
```

```
0B43 22 20 0F          6220          SHLD    BBUF        ;SAVE MEMORY LOC
0B46 CD 0A 06          6225          CALL    CRLF        ;FOR NEATNESS
0B49 21 71 05          6230          LXI     H,VPREM     ;'VERIFY ERROR' MESSAGE
0B4C CD 52 01          6235          CALL    STRO        ;WRITE IT OUT
0B4F CD AC 05          6240          CALL    WRBB        ;WRITE MEMORY LOC
0B52 3A 35 0F          6245          LDA     DBUF+5      ;GET TAPE DATA
0B55 CD D9 05          6250          CALL    HOUT        ;WRITE IT OUT
0B58 CD D3 05          6255          CALL    SPO1        ;SPACE
0B5B 3A 36 0F          6260          LDA     DBUF+6      ;GET MEMORY DATA
0B5E CD D9 05          6265          CALL    HOUT        ;WRITE IT OUT
0B61 CD 0A 06          6270          CALL    CRLF        ;MORE NEATNESS
0B64 C3 56 00          6275          JMP     ABRT        ;ABORT
0B67                   6280 *  ********************
0B67                   6285 *  CYCLIC REDUNDANCY CHECK   ( X^16 + X^12 + X^5 + 1 )
0B67                   6290 *  ********************
0B67 D5                6295 CRCX     PUSH    D           ;SAVE (DE)
0B68 A9                6300          XRA     C           ;COMPUTE CRC
0B69 57                6305          MOV     D,A         ;
0B6A 0F                6310          RRC                 ;
0B6B 0F                6315          RRC                 ;
0B6C 0F                6320          RRC                 ;
0B6D 0F                6325          RRC                 ;
0B6E E6 0F             6330          ANI     0FH         ;
0B70 AA                6335          XRA     D           ;
0B71 5F                6340          MOV     E,A         ;
0B72 0F                6345          RRC                 ;
0B73 0F                6350          RRC                 ;
0B74 0F                6355          RRC                 ;
0B75 57                6360          MOV     D,A         ;
0B76 E6 1F             6365          ANI     1FH         ;
0B78 A8                6370          XRA     B           ;
0B79 4F                6375          MOV     C,A         ;
0B7A 7A                6380          MOV     A,D         ;
0B7B E6 E0             6385          ANI     0E0H        ;
0B7D AB                6390          XRA     E           ;
0B7E 47                6395          MOV     B,A         ;
---
0B7F 7A                6400          MOV     A,D         ;
0B80 0F                6405          RRC                 ;
0B81 E6 F0             6410          ANI     0F0H        ;
0B83 A9                6415          XRA     C           ;
0B84 4F                6420          MOV     C,A         ;CRC IN (BC) COMPLETE FOR THIS BYTE
0B85 D1                6425          POP     D           ;RESTORE (DE)
0B86 C9                6430          RET                 ;
0B87                   6435 *  ********************
0B87                   6440 *  BYPASS REMAINDER OF RECORD
0B87                   6445 *  ********************
0B87 CD D9 0B          6450 BPDT     CALL    CSIP        ;READ REC LN (LOW)
0B8A 4F                6455          MOV     C,A         ;
0B8B CD D9 0B          6460          CALL    CSIP        ;READ REC LN (HI)
0B8E 47                6465          MOV     B,A         ;INTO (BC)
0B8F CD D9 0B          6470          CALL    CSIP        ;READ PAST LOAD ADDRESS
0B92 CD D9 0B          6475          CALL    CSIP        ;
0B95 CD D1 0C          6480 BPD1     CALL    CSIH        ;READ PAST DATA
0B98 0B                6485          DCX     B           ;REC LN COUNT
0B99 79                6490          MOV     A,C         ;
0B9A B0                6495          ORA     B           ;THAT ALL ?
0B9B C2 95 0B          6500          JNZ     BPD1        ;NO.  EAT MORE
0B9E CD D9 0B          6505          CALL    CSIP        ;GET PAST CRC
0BA1 CD D9 0B          6510          CALL    CSIP        ;GET PAST CRC
0BA4 CD AA 0B          6515          CALL    RRGP        ;READ THE RECORD GAP
0BA7 C3 52 09          6520          JMP     CLOH        ;READ MORE RECORDS
0BAA                   6525 *  ********************
0BAA                   6530 *  READ RECORD GAP CHECK
0BAA                   6535 *  ********************
0BAA D5                6540 RRGP     PUSH    D           ;SAVE (DE)
0BAB CD 1D 06          6545 RRG1     CALL    ESCP        ;WANT BYE BYE ?
0BAE 16 20             6550          MVI     D,20H       ;MINIMUM LENGTH RECORD GAP
0BB0 CD 01 0C          6555          CALL    CSIH        ;READ A BYTE
0BB3 5F                6560          MOV     E,A         ;SAVE DATA BYTE
0BB4 CD 01 0C          6565 RRG2     CALL    CSIH        ;READ ANOTHER
0BB7 BB                6570          CMP     E           ;SAME ?
0BB8 C2 AB 0B          6575          JNZ     RRG1        ;RETRY
0BBB B7                6580          ORA     A           ;ZEROS GAP ?
0BBC CA C3 0B          6585          JZ      RRG3        ;YES.  LONG ENOUGH
0BBF 3D                6590          DCR     A           ;NO.  A ONES GAP ?
0BC0 C2 AB 0B          6595          JNZ     RRG1        ;NO.  GARBAGE DOUBLE DATA.  RETRY
0BC3 15                6600 RRG3     DCR     D           ;YES.EITHER ONES OR ZEROS
0BC4 C2 B4 0B          6605          JNZ     RRG2        ;NEED A BUNCH
0BC7 D1                6610          POP     D           ;RESTORE (DE)
0BC8 C9                6615          RET                 ;FOUND A GAP
0BC9                   6620 *  ********************
0BC9                   6625 *  CASSETTE END OF TAPE
0BC9                   6630 *  ********************
0BC9 CD 0A 06          6635 CEOT     CALL    CRLF        ;MAKE IT NEAT
---
0BCC 21 D5 0B          6640          LXI     H,EOTM      ;POINT TO MESSAGE
0BCF CD 52 01          6645          CALL    STRO        ;WRITE MESSAGE
0BD2 C3 56 00          6650          JMP     ABRT        ;ABORT
0BD5 45 4F 54          6655 EOTM     ASC     'EOT'
0BD8 0D                6660          DB      13
0BD9                   6665 *  ********************
0BD9                   6670 *  READ CASSETTE DATA TRUE / COMPLIMENT PAIR
0BD9                   6675 *  ********************
0BD9 C5                6680 CSIP     PUSH    B           ;SAVE (BC)
0BDA CD 01 0C          6685          CALL    CSIH        ;GET TRUE
0BDD 47                6690          MOV     B,A         ;SAVE DATA
0BDE CD 01 0C          6695          CALL    CSIH        ;GET COMPLIMENT
0BE1 2F                6700          CMA                 ;MAKE IT TRUE
0BE2 B8                6705          CMP     B           ;CHECK IT
0BE3 C1                6710          POP     B           ;RESTORE (BC)
0BE4 C2 E8 0B          6715          JNZ     HDER        ;BOO !  A HEADER ERROR
0BE7 C9                6720          RET                 ;AHH GET TO IT
0BE8                   6725 *  ********************
0BE8                   6730 *  HEADER ERROR MESSAGE
0BE8                   6735 *  ********************
0BE8 CD 0A 06          6740 HDER     CALL    CRLF        ;HEADER ERROR
0BEB 21 F4 0B          6745          LXI     H,HDEM      ;POINT TO ERROR MESSAGE
0BEE CD 52 01          6750          CALL    STRO        ;WRITE IT OUT
0BF1 C3 56 00          6755          JMP     ABRT        ;ABORT
0BF4 48 45 41 44       6760 HDEM     ASC     'HEADER ERROR'
     45 52 20 45
     52 52 4F 52
0C00 0D                6765          DB      13
0C01                   6770 *  ********************
0C01                   6775 *  CASSETTE INPUT HANDLER
0C01                   6780 *  ********************
0C01 CD 1D 06          6785 CSIH     CALL    ESCP        ;WANT OUT ?
0C04 DB 6F             6790          IN      CMSC        ;READ STATUS
0C06 E6 10             6795          ANI     10H         ;READY BIT FOR INPUT
0C08 C2 01 0C          6800          JNZ     CSIH        ;READY=0
0C0B DB 6F             6805          IN      CMSD        ;READ THE DATA
0C0D C9                6810          RET                 ;THAT'S IT
0C0E                   6815 *  ********************
0C0E                   6820 *  WRITE TAPE MARK FOR END OF TAPE - EOT
0C0E                   6825 *  ********************
0C0E 3E 3C             6830 MEOT     MVI     A,3CH       ;START BYTE
0C10 CD 33 09          6835          CALL    CSOH        ;
0C13 3E E6             6840          MVI     A,0E6H      ;SYNC BYTE
0C15 CD 33 09          6845          CALL    CSOH        ;
0C18 3E 54             6850          MVI     A,'T'       ;TAPE MARK - EOT
0C1A CD 2B 09          6855          CALL    CSOF        ;CASSETTE OUTPUT
0C1D 0E 15             6860          MVI     C,15H       ;PATTLEN FOR TAPE END
0C1F CD 2B 09          6865 MET1     CALL    CSOF        ;CASSETTE OUTPUT
---
0C22 0D                6870          DCR     C           ;DECR COUNT
0C23 C2 1F 0C          6875          JNZ     MET1        ;MORE
0C26 C9                6880          RET                 ;DONE
0C27                   6885 *  ********************
0C27                   6890 *  CASSETTE TIMEOUT ERROR MESSAGE
0C27                   6895 *  CASSETTE INTERFACE DID NOT RESPOND
0C27                   6900 *  ********************
0C27 CD 0A 06          6905 CSTO     CALL    CRLF        ;NEAT AGAIN
0C2A 21 33 0C          6910          LXI     H,CSTM      ;POINT TO MESSAGE
0C2D CD 52 01          6915          CALL    STRO        ;WRITE IT OUT
0C30 C3 56 00          6920          JMP     ABRT        ;ABORT
0C33 43 41 53 53       6925 CSTM     ASC     'CASSETTE TIMEOUT
     45 54 54 45
     20 54 49 4D
     45 4F 55 54
0C43 0D                6930          DB      13
0C44                   6935 *  ********************
0C44                   6940 *  WRITES MESSAGE 'CRC ERROR'
0C44                   6945 *  ********************
0C44 CD 0A 06          6950 CRCE     CALL    CRLF        ;NEATNESS COUNTS
0C47 21 50 0C          6955          LXI     H,CRCM      ;POINT TO MESSAGE
0C4A CD 52 01          6960          CALL    STRO        ;WRITE IT OUT
0C4D C3 56 00          6965          JMP     ABRT        ;ABORT
0C50 43 52 43 20       6970 CRCM     ASC     'CRC ERROR'
     45 52 52 4F
     52
0C59 0D                6975          DB      13
```

SOFTWARE PROGRAM LIBRARIES

By Robert A. Stevens

INTRODUCTION

Hundreds of microcomputer programs—The following list some of the hundreds of source programs that are available to members of Intel's and Motorola's users' group program libraries.

INTEL'S 8080 USER'S PROGRAM LIBRARY

Hundreds of microcomputer source code programs are available on paper tape and in listing form through INSIGHT™ user's library run by the Microcomputer Systems Division of Intel Corporation.

INSITE

Insite™ (Intel Software Index and Technology Exchange) software library is operated as an industry service by INTEL. INSITE™ is an outgrowth of the Intel Microcomputer User's Library of general-purpose microcomputer programs to the library for several years. It now contains over 200 programs for 8080 and 8008 8-bit microcomputers and over 100 programs for 4040 and 4004 4-bit microcomputers.

Intel's 8080 Users Library offers the following services. As a member you have access to:

- Over 200 Programs in the Program Library Manual.
- Source Paper Tapes and Listings for all programs in the Library at a minimal reproduction fee.
- Updates of new programs sent to you every other month during the term of your membership. You must return your Registration Card to insure that you are on the "Update" mail list.
- A one year membership extension of 5 free tapes will be awarded for every program submitted and accepted for inclusion to Insite.

The Library encourages you to take advantage of the many available services. If you have any questions call the Insite Administrator, Mary Anne Vilas, at #408/246-7501 ext. 2948.

LIBRARY PROGRAM MANUAL

A Program Library Manual contains all programs with listings up to three pages long. Programs longer than three pages will be described in authors' abstracts. Update packages for the manual, containing newly received programs, will be published every other month.

PAPER TAPE COPIES

Paper tapes containing source code for each of the programs in the library will be made available on request. A prepaid handling fee of $15 will be charged for each source tape. As a bonus, new members will receive five free source tapes of their choice when they return their registration card.

MEMBERSHIP

A one year membership in the library is free to persons who contribute acceptable programs. The membership fee for other persons is $100 annually. Members will receive the program library manual and update packages during the term of their membership.

SEND COPY OF PROGRAMS TO *INTERFACE AGE*

Software Editor's note: If you submit a program to the INTEL user's library, also (at the same time) submit a copy of your paper tape source code and short descriptive write up to INTERFACE AGE for publication and get paid for your effort. INTERFACE AGE pays $15.00 to $30.00 per typeset page for original Microcomputer software programs. All programs submitted to INTERFACE AGE for publication will be put in the free public domain vie the Microcomputer Software Depositary for low cost distribution. Send all software programs to Robert A. Stevens, Software Editor, INTERFACE AGE.

INTEL 8080 PROGRAM INDEX

3-Byte Positive Fractional Multiply
8-Bit Multiply and Divide
8-Bit Random Number Generator
16-Bit 2's Complement Signed Multiplication
16-Bit CRC for Polynomial X16 + X12 + X5 + 1
16-Bit Division—16-Bit Result
16-Bit Division—16-Bit Result
16-Bit Multiply—16-Bit Result
16-Bit Multiply—16-Bit Result
16-bit Multiply—32-Bit Result
16-Bit Random Number Generator
16-Bit Square Root Routine
32-Bit Binary to BCD Conversion, Leading Zero Blanking
32-Bit Divide Subroutine
4040 Cross Assembler for Intellec 8/MOD 80 and MDS-800
8008 Cross Assembler for HP 3000
8008 Cross Inverse Assembler for HP 2100
8008 Disassembler
8008 MACRO Definition Set for Assembly on PDP-11
8080 Cross Assembler for HP 3000
8080 Cross Assembler for HP 2100 DOS

8080 Disassembler
8080 Disassembler
8080 Floating Point Extended Math Package
8080 Floating Point Package with BCD Conversion Routine
8080 Idle Analyzer for Approximating CPU Utilization
8080 I/O System Status Display
8080 Least Squares Quadratic Fitting Routine
8080 RAM Memory Test
8080 Symbol Table Dump

A/D Converter Routine
Adaptive Game Program
Algebraic Compare Subroutine
APL Graphic Display on a 5 X 7 Dot Matrix
Approximating Routine
ASCII Display
Absorbance Calculation
Assembler Oriented Centronics 306 Line Printer Handler and Error Only Assembler
Banner Print and Punch
BASIC CPU State Vector Maintenance
Basic Digital Panel Meter Call
BASIC Interpreter
BASIC/M Translator and Interpreter
BCD to BIN Conversion Routine
BCD to/from Binary Conversion
BCD Input and Direct Conversion to Binary Routine
BCD Multiplication
BCD Sum for 8008
BCD Up/Down Counter
BIN to BCD Conversion Routine

Binary to BCD Subroutine
Binary to HEX Routine
Binary Loader for MDS
Binary Multiplication—24-Bit
Binary Search
Binary Search Routine
BINDECBIN—Binary to/from BCD
BINLB—8080 System Loader
Blackjack
$BLPT
BOOT—Bootstrap Loading and Program Patching

Calendar Subroutine
Character Interpreted Memory Dump
Clock Subroutine
Compare
Compare Object Code Tape with Memory
Control Data Output
CRECH—Cyclic Redundancy Check
Cross Assembler for PDP-11
Cross Assembler for PDP-11
Cross Assembler for Nova 1200
Cross Assembler for Nova 1220, IBM 360/40 and CDC 3000
Cross Assembler for Varian Data Machine
CRTBZ—GET
Cyclic Redundancy Character Generator
Cyclic Redundancy Check
Cyclic Redundancy Check for Data String of 2^{16} Bytes
Data Array Move
Data I/O PROM Processor
Decrement H and L Registers
Delete Comments
Diagnostic 1003—Memory Validity Check
Digital to Analog Conversion for Eight Outputs
Dissambler
Disk Dump Routine for ICOM F DOS-11/MOD 80 Floppy DOS
Double Precision Integer Arithmetic Package
Double Precision Multiply

Elementary Function Package
ERLIST
Examin

Factorial of a Decimal Number
Fast Floating Point Square Root Routine
Fixed and Floating Point Arithmetic Routines
Fixed Point CHEBYSHEV Sine and Cosine for PL/M Users
Flag Processing Routine
Floating Point Format Conversion Package
Floating Point Math Package
Floating Point Package for Intel 8008 and 8080 Microprocessors
Floating Point Procedures
Floating Point Square Root

Gambol
Game of Life
Generalized Stepper Motor Drive Program
Gray to Binary Conversion

Handler for Tally PTP
HEX Convert—Convert Intel HEX Format to Prolog HEX File Converter
HEX to Decimal Conversion
HEX Format Paper Tape Dump for SDK
HEX Tape Loader for SDK
High Speed Paper Tape Reader with Stepper Motor Control

IBM Selectric Output Program
ICE-80 Disassembler
I-Command—Insert Data in HEX Form from TTY into RAM
Input/Output Commands for MDS
Intellec 8/MOD 80—Silent 700 Interface
Interfacing the MDS and HP 2644A
Interrupt Driven Clock Routine
Interrupt Handler (Re-Entrant)
Interrupt Service Routine
I/O Simulation MACROS

K, Program Trap and Dump Routine
Kalah

Legible Paper Tape
List
Lewthwaite's Game
List Device Program
List 1—High Speed List Program for Intellec 8
LIst/Print/Type "List SRC" on Diskette
Log Base 2

Mastermind
Match Game
Maze
Maze
Memory Compare
Memory Diagnostic Program
Memory Dump
Memory Test for the 8080
Memory Test Program
Model 101 Centronics Printer Handler
Mon 256—256-Byte PROM Monitor
Morse Code Generator
MUL/DIV Multi-Precision Pack for 8080

Natural Logarithm
N-Byte Binary Multiplication and Leading Zero Blanking
Nim
Nim
Nova Cross Assembler—Intel 8080
Numbers

Octal Code Conversion for PDP-11
Octal Debugging Program (ODT) for the MCS-80 Computer
Octal PROM Programming

Page Break for Tektronix 4010 I/O Graphics Terminal
Page Listing Program
Paper Tape Reformatter for SDK

Pass—Parameter Passing Routine
PDP-11 Binary File to Intel HEX File Converter
PL/M 80 Pass 3
PL/M Floating Point Interface
PL/M Histogram Procedure and Random Number Generator
PROM Programmer for Intellec 8
Proportional Power Control Image Builder
Punch Binary Tape
Punch Test or TTY Reader/Punch Test

RAM Check
RAM Test Program
RANDOM$BITS
Random Number Generator—RNGEN
Read and Interrupt Modifications for Intellec 8/MOD 80
Reader Test
Read/Write Routines for Interchange Tapes
Real Time Executive
RMSTF—Integration Routine
Run 0

Save/Restore CPU State on an Interrupt
SDK-80 Keyboard Monitor
Shellsorting Routine
Sin X, Cos X Subroutine
SMAL: Symbolic Microcontroller Assembly Language
Software Stack Routines for 8008
Source Paper Tape to Magnetic Cassette
SQRTF—Calculates 8-Bit Root of 16-Bit Number
State 2
Structured Assembler for 8080
Subroutine DMULT (Decimal Multiplication)
Subroutine Log—Common Logarithms
Subroutine SQRT
Symbol Table Dump for Intellec 8/MOD 80
Symbol Table List Routine

Tally—Use Tally 2200 Line Printer in Assembly Stage of Programming
Tally R2050 HSPTR Driver
Tape Duplicator
Tape Labeler for MDS
Teleprocessing Buffer Routine
Terminal Editor
Text Storage Program
Tic-Tac-Toe
Time Sharing Communications
TIMIT—Interrupt Driven Real Time Clock Routine
T.I. Silent 700 Interface—Intellec MDS
TRACE—Program Trace and Debugger
Trace Routine
TTY Binary Dump Routine
TTY Binary Load Routine
Type

Quicksort Procedures

Video Driver

Work Game, The

MOTOROLA'S M6800 USER'S GROUP LIBRARY

M6800 User's Group Formed

The M6800 Microprocessor User's Group has been formed by Motorola's MicroSystems Group to facilitate and promote the sharing of information among M6800 Family users. Two forms of information are offered, the User's Group Library and the User's Group "DataGram" Newsletter.

User's Group Library

The library is a repository of over 65 M6800 programs available to all User's Group member to save the time and expense of reinventing the same software "wheels". Program distribution includes a ring binder with source listings of most library programs. Longer programs, those listings over five pages, are described in the standard program distribution, with source listings available on request for a nominal service charge.

"DataGram" Newsletter

"DataGram" will include information about new library entries, new Motorola microprocessor hardware and software products, and ideas of general interest to members.

Membership Information

Motorola M6800 User's Group membership provides library updates and newsletters for a two year period.

Anyone submitting a suitable entry for the program library automatically receives a free two-year membership. Programs should be of general interest and should be documented on an M6800 User's Group Library Submittal form. Although membership via program submittal is encouraged, memberships may also be purchased for $100.00 each.

Additional User's Group information is available from: MicroSystems Group, Motorola Semiconductor Products Inc. P.O. Box 2953 MD56104 Pheonix, Az. 85036 or Telephone: (602) 244-6331.

Send Copy of Program to INTERFACE AGE

Software Editor's note: If you submit a program to the INTEL user's library, also (at the same time) submit a copy of your paper tape source code and short descriptive write up to INTERFACE AGE for publication and get paid for your effort. INTERFACE AGE pays $15.00 to $30.00 per typeset page for original Microcomputer software programs. All programs submitted to INTERFACE AGE for publication will be put in the free public domain vie the Microcomputer Software Depositary for low cost distribution. Send all software programs to Robert A. Stevens, Software Editor, INTERFACE AGE.

M6800 USER GROUP LIBRARY PROGRAM INDEX

Program Number	Program Name & Description
1.	EXBUG ROUTINE CBCDHX—Convert a Hexadecimal character to a binary number.

MICROPROCESSOR COMPONENTS

CPU'S

8008-1 (18 Pin)	8 Bit CPU (PMOS)	$17.95
8080A (40 Pin)	8 Bit CPU (2us) (NMOS)	24.95

8080 SUPPORT DEVICES

8212	8 BIT I/O Port	$ 4.25
8214	Priority Interupt Control	8.95
8216	Bi-Directional Bus Driver	4.25
8224	Clock Generator	8.00
8255	Programmable Peripheral Interface	12.00

ROM'S

74S387	1024 Bit Programmable	$ 2.50
MM5230	2048 Bit	1.95
DM8796	4096 Bit	10.00

PROM'S

82S23	32 x 8 Open Collector (Schottky)	$ 3.00
1702 A	2048 Bit (256 x 8) (1us) Erasable and Electrically Reprogrammable	5.00
1702AL	2048 Bit (256 x 8) (LO-PWR) (1us) Erasable and Electrically Reprogrammable	7.00
2708	8192 Bit (1024 x 8) Erasable and Electrically Reprogrammable	40.00
8223	32 x 8 Open Collector	3.50

SHIFT REGISTER'S

MM506N	Dual 100 Static	$ .89
P-2405	1024 Dynamic	4.95
N2518B	Hex 32 Bit	3.95
N2533V	1024 Static	3.95
MM5013N	1024 Bit Accumulator Dynamic	2.00
MM5017N	Dual 500/512 Dynamic	2.00
MM5058	1024 x 1 Static	2.50
TMS3002LR	Dual 50 Static	3.00
TMS3132NC	Dual 144 Static	2.00

CALCULATOR CHIPS

MM5736	6 Digit Cal.	$1.25
CT5001	12 Digit Cal. *With Specifications*	1.75

RAM'S

21L02	1024 x 1 Static	$1.58
1101	256 x 1 Static	1.00
1103	1024 x 1 Dynamic	1.50
2101	256 x 1 Static (1us)	3.00
2102	1024 x 1 Static (1us)	1.50
2102-1	1024 x 1 Static (500NS)	1.65
2107B	4096 x 1 Dynamic (200NS)	6.50
2107B-4	4096 x 1 Dynamic (270NS)	5.00
2107B-6	4096 x 1 Dynamic (350NS)	4.50
3107	256 x 1 Static (80NS)	2.95
3107A	256 x 1 Static (60NS)	3.50
4050NL	4096 x 1 Dynamic (300NS)	4.00
5261	1024 x 1 Dynamic (400NS)	3.00
5262	2048 x 1 Dynamic (365NS)	3.00
5280	4096 x 1 Dynamic (200NS)	4.00
7489	16 x 4 Static	1.50
8599	16 x 4 Static	1.50

MISC. OTHER COMPONENTS

N8T20	Bi-Direc-tional One Shot	$4.00
N8T26	Quad Bus Driver/Receiver	3.25
N8T97	Tri-State Hex Buffer	1.45
1488	RS232 Quad Line Driver	1.25
1489	RS232 Quad Line Receiver	1.25
D3207A	Quad Bi-Polor to MOS Level Shifter/Driver	2.50
C-3404	6 Bit Latch 12NS Output Delay	3.95
P-3408A	Hex Sense Amplifier W/Latch	6.75
P-4201	Clock Generator	4.95
MM-5320	T.V. Camera Sync. Generator	6.00
MM-5369	Oscillator Pre-scaler	2.00
MC-6850L	Asynchronous	
DM8130N	Ten Bit Comparator	2.25
DM8131N	6 Bit Comparator	2.00

DISPLAY LED'S

Type	*Polarity*	*HGT.*	*Price*
MAN-4	Common Cathode	.187	$ .75
ILD-74	Logic Drive	(8 Pin)	
	Opto-Isolator	(8 Pin)	1.00
DL-707	Common Anode	.300	1.25
DL-747	Common Anode (Jumbo)	.60	2.00
TIL-113	Opto Coupler	(6 Pin)	2.00
TIL-302	Common Anode (LORR DEC)	.27	1.00

TTL PRODUCT

7400	.14	7441	.85	7496	.65	74160	.86
7401	.20	7442	.44	7497	2.00	74161	.62
7402	.20	7443	1.20	74100	1.25	74162	1.00
7403	.20	7445	.89	74107	.76	74163	.76
7404	.20	7446	.87	74109	.35	74164	.80
7405	.20	7447	.69	74110	.50	74165	.90
7406	.39	7448	.81	74116	2.00	74166	1.00
7407	.39	7450	.20	74120	1.25	74167	3.00
7408	.20	7451	.20	74121	.34	74170	2.00
7409	.24	7453	.20	74122	.39	74172	9.72
7410	.20	7454	.20	74123	.50	74173	1.25
7411	.20	7460	.20	74125	.45	74174	.85
7412	.24	7470	.20	74126	.45	74175	.75
7413	.35	7472	.23	74128	.65	74176	.85
7414	.70	7473	.26	74132	.95	74177	.85
7416	.33	7474	.29	74136	.50	74180	.75
7417	.33	7475	.39	74141	.80	74181	2.00
7420	.20	7476	.31	74142	4.00	74182	.90
7422	.50	7479	1.50	74143	3.00	74184	1.65
7423	.28	7480	.69	74144	4.00	74185	1.30
7425	.24	7482	.72	74145	.70	74186	5.00
7426	.24	7483	.75	74147	2.50	74190	1.00
7427	.24	7485	.90	74148	1.75	74191	.65
7428	.40	7486	.25	74150	1.00	74192	.85
7429	.40	7488	3.50	74151	.70	74193	.85
7430	.20	7489	1.50	74153	.70	74194	1.20
7432	.28	7490	.39	74154	.90	74195	.55
7433	.34	7491	.65	74155	.70	74196	.80
7437	.28	7492	.39	74156	.90	74198	1.50
7438	.28	7493	.39	74157	.70	74199	1.75
7439	.36	7494	.70	74158	1.75	74200	3.50
7440	.20	7495	.50	74159	2.25	74279	1.75

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2. EXBUG ROUTINE INCHMP—Input character with no parity.
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10. M6800 RESIDENT I/O PACKAGE—EXBUG VERSION (MEXRIO)—I/O routines for use with the Resident Editor and Resident Assembler utilizing EXBUG 1.1 or 1.2.
11. M6800 RESIDENT I/O PACKAGE—MIKBUG VERSION (MKRIO)—I/O routines for use with the Resident Editor and Resident Assembler utilizing MIKBUG Revision 9.
12. MPU INSTRUCTION TEST—To insure the operation of the instruction set.
13. MEMORY TEST—To test memory. To verify that a particular data pattern can be written to a specific location and read back error free.
14. PIA TEST—Test program to functionally verify the EXORcisor I/O Module (or PIA's).
15. 32 BIT RE-ENTRANT FLOATING POINT MULTIPLY—Takes two 32 bit floating point numbers and multiplies them. No normalization is attempted. Exponent overflow is not detected.
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17. HIGH DENSITY TAPE PUNCH—Punches a properly formatted binary paper tape from memory for loading with the biload program.
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20. TIC-TAC-TOE—Allows an operator to play the game of Tic-Tac-Toe at the EXORciser console device.
21. "PUNCH" FOR DATA I/O PROM PROGRAMMER—Punches a paper tape from any starting address in memory to any finish address.
22. BCD TO BINARY CONVERSION—Convert four BCD digits to their binary equivalent.
23. SQUARE ROOT OF A 16 BIT NUMBER—Program finds square root of a 16 bit number.
24. UPC (UNIVERSAL PRODUCT CODE) LABEL CONVERSION—Decodes the Universal Product Code symbol found on grocery store labels when scanned with an optical wand.
25. ASCII DATA TO MORSE CODE CONVERSION—Take ASCII data from the keyboard of the EXORciser and convert it to morse code.
26. 32 BIT FLOATING POINT PACKAGE—Subroutines for adding, subtracting, multiplying and dividing floating point numbers of a specified format.
27. RANDOM NUMBER GENERATOR—Generates a (Pseudo) random sequence of 16 bit binary numbers R(n) using a linear congruential sequence.
28. "PUNCH" FOR PROLOG SERIES 90 PROM PROGRAMMER—To generate a formatted tape for the PROLOG series 90 PROM programmer for programming type 2708 Erasable PROM's.
29. M6800 REAL TIME OPERATING SYSTEM—A real-time operating system for the Motorola M6800 Microprocessor.
30. BLACKJACK—Exorciser Deals Blackjack.
31. BINARY TO BCD CONVERSION—Converts a 16-bit binary number (unsigned) to packed BCD 5-digit (3 byte).
32. DECIMAL ARITHMETIC PACKAGE—This is a group of 8 multiple-precision BCD arithmetic subroutine. These subroutines are integer and floating point addition, subtraction, multiplication and division. Also included is a subroutine to move the numbers to and from the scratchpad (operations: A + C, A – C, A*B and C/A).
33. DELAY SUBROUTINE—To generate a delay from 1 → 65, 536 milliseconds. To test a PIA bit (for either a one or a zero) until either the test is met or a timeout occurs.

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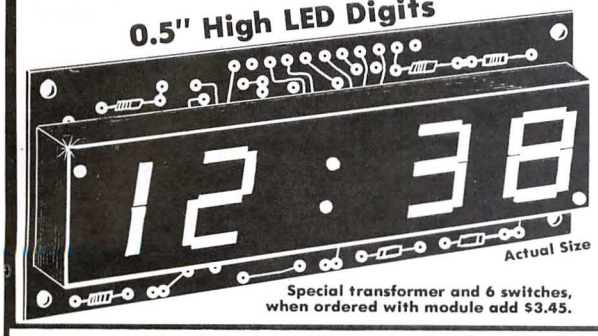

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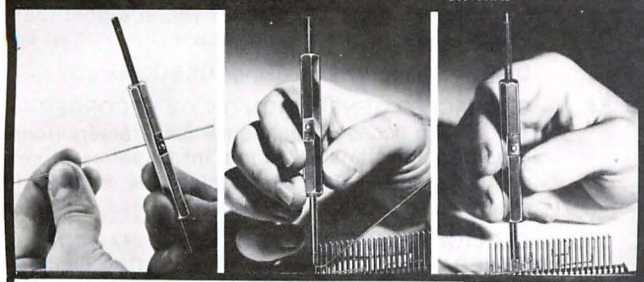

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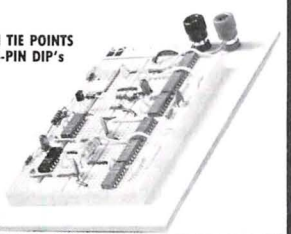

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3.3/50V . . .08	.65/10	100/16V . . .11	.85/10	470/25V . . .29	2.35/10
4.7/35V . . .08	.65/10	100/25V . . .13	1.10/10	1000/10V . .24	1.96/10
4.7/50V . . .08	.68/10	100/50V . . .21	1.71/10	1000/16V . .29	2.35/10
10/16V 08	.65/10	220/10V . . .13	1.08/10	1000/25V . .42	3.33/10
10/25V 08	.65/10	220/16V . . .15	1.16/10	2200/10V . .42	3.33/10
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3.3/35V . . .12	.95/10	47/16V . . .14	1.15/10	470/16V . . .32	2.55/10
3.3/50V . . .12	1.00/10	47/25V . . .17	1.30/10	470/25V . . .37	3.00/10
4.7/25V . . .11	.90/10	47/50V . . .21	1.17/10	1000/16V . .33	2.65/10
4.7/35V . . .12	.95/10	100/10V . . .14	1.13/10	1000/16V . .39	3.15/10
4.7/50V . . .12	1.00/10	100/16V . . .17	1.30/10	1000/25V . .56	4.50/10
10/25V 12	1.00/10	100/25V . . .20	1.55/10	2200/10V . .50	3.96/10
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33/16V 12	1.00/10	220/50V . . .40	3.23/10	10000/10V 1.15	9.19/10
		330/10V . . .14	1.16/10		

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7412 .21	7495 .70	74196 .88	4024 .84	LM340T-8 1.25
7413 .25	7496 .70	74197 .88	4025 .23	LM340T-12 1.25
7414 .89	74100 1.28	74198 1.49	4026 1.68	LM340T-15 1.25
7416 .25	74107 .30	74199 1.49	4027 .40	LM340T-18 1.25
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7420 .21	74121 .35	74279 .55	4029 1.14	LM3900N .88
7421 .25	74122 .44	74365 .67	4030 .23	LM3909N .69
7423 .35	74123 .61	74366 .67	4033 1.51	MC1456V 1.00
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7433 .30	74148 1.30	8097 .67	4044 .70	NE560B 3.83
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7438 .25	74151 .70	75150 1.16	4049 .40	NE562B 3.83
7440 .21	74153 .65	75450 .88	4050 .40	NE565A 1.25
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1N5232B 5.6v .15 $11/C	1N5242B 12v .15 $11/C
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34. OFFSET LOAD MEMORY FROM TAPE—Load memory from paper tape reader (ASR 33) at a location in memory at a constant offset location from that specified on the tape.

35. BNASC—This subroutine converts an unsigned 16-bit number from binary to ASCII of any base between 2 and 16.

36. CHRISTMAS CARD LIST—Prints Address labels. Provision for index, loading, verification, and deletion of individual label.

37. RE-ENTRANT ASCII TO BAUDOT CONVERTER SUBROUTINE (ASTOBAUD)—Converts ASCII characters to their BAUDOT equivalents including shift codes.

38. TEXT STRING (TXTSTG)—A text string is input via keyboard followed by EOT (CTRL/D) delimiter. The text string is then printed repeatedly. Exit is by CPU RESET. Useful as I/O checkout, general system functioning, and effective for demonstrations.

39. DUMP/HEX/DISPLAY—Dumps a block of memory in hex and display mode. Can be called as a subroutine or driven from the control console.

40. HANGMAN—This is a game in which the computer selects a word from a programmed list of words. The selection is randomized. The player then enters guesses of letters in the word. The game is completed when the work is correctly identified, or when eight incorrect guesses result in display of the entire HANGMAN!

41. MEMORY DUMP ON DISKETTE (FDISK)—Dump the contents of memory onto an EDOS2 structured diskette in the Motorola defined format (S0, S1, S9).

42. VERIFY PAPER TAPE COPIES (TAPVRF)—Compares paper tape copies punched in any format with the original paper tape.

43. DEBUG—Debug package for M6800. The package provides commands for: examine and/or change of memory locations, examine and/or change of processor registers, step-by-step program execution, input of binary formatted paper tape on Teletype Reader.

44. TOWERS OF HANOI SOLUTION—Solves the "Towers of Hanoi" puzzle for up to 9 discs. Was written to demonstrate how to write recursive programs on the M6800.

45. WL* (WIRE LISTER)—Creates, edits, and prints a file of signal names and pin coordinates from PC board. The print-out could be used in an automatic wire-wrapping system.

46. NON-LINEAR CONVERSION TABLES (CVTBLS)—This program converts any X value between 0 and 10, 240 to a Y value between 0 and 10,240. The conversion utilizes look-up tables of 11 Y values, with a linear interpolation between them.

47. ASSEMBLER/EDITOR INTERNAL TRANSFER ROUTINE (EXBUG)—AETX.1—This program, when loaded after the co-resident Assembler/Editor software, allows internal two-way transfer between the Assembler and Editor without the external tape transfers otherwise needed. Edit buffer and assembler symbol table are separately maintained.

48. ASSEMBLER/EDITOR INTERNAL TRANSFER ROUTINE (MIKBUG)—AETM.1—This program, when loaded after the co-resident Assembler/Editor software, allows internal two-way transfer between the Assembler and Editor without the external tape transfers otherwise needed. Edit buffer and Assembler symbol table are separately maintained.

49. TRACE—Trace is a subroutine which the user jumps to at various "test points" is a new undebugged program for the purpose of printing out the address followed by the contents of the A and B registers. This allows tracing of the flow of the new program up to the point at which it 'blows'.

50. 24 BIT RE-ENTRANT FLOATING POINT PACKAGE—(1) addition; (2) subtraction; (3) multiplication; (4) division; (5) float; (6) fix to 16 bit integer; (7) negate; (8) clear; (9) copy; (10) compare*; (11) string to flt pnt*; (12) fit pnt to string* *—not re-entrant

51. RDR1.B—Ram memory loader for Motorola format hex paper tape using 300 char/sec reader. Loads memory with a single program and halts.

52. MISSIONARIES AND CANNIBALS (MISCAN)—The object of the game is to move three missionaries and three cannibals across a river, in a boat that can only accommodate two people.

53. DUMP—Memory dump using MIKBUG for I/O

54. CHARACTER GENERATION ON X-Y RECORDER—The system accepts alphanumeric characters from keyboard and translates them into a series of x-y displacements voltages, forming the shape of entered character on x-y recorder.

55. CYCLIC REDUNDANCY CHECK CHARACTER GENERATOR—Calculation of the CRCC of a data buffer stored in locations Bebuffer-Ebuffer.

56. DECODE—Provides the convenience of a "backwards" assembler; that is, given a machine-resident block of object code the program will analyze it and provide a pseudo-source listing of the code.

57. PRTMSG—A re-entrant message printing routine.

58. DISK FILE TRANSFER—To give EXORciser users with single drive unit EXORdisks the capability to copy a file from one diskette to another without using paper tape or cassette as intermediate media.

59. QUICK LOAD (QLOAD)—Loads an EXORciser format object tape into memory without stopping the tape after each record. Will detect and indicate checksum and no change errors.

60. M6800 RESIDENT I/O PACKAGE—MINIBUG II VERSION (M2RIO)—I/O routines for use with the Resident Editor and Resident Assembler utilizing Minibug II.

61. MPL CORE SORT PROGRAM—Sorts data arrays in ascending order. Data array can be either BINARY (1) or BINARY (2) and a data entry can be of arbitrary length. The sort is done in place.

62. MEMORY TEST/EVALUATION MODULE II—To test memory. To verify that a particular data pattern can be written to a specific location and read back error free. The test is run using the evaluation module utilizing MINIBUG I/O routines.

63. TTYIO—This is an input-output sub-routine. It will output a defined character string or store a character string in a defined buffer (location).

64. TELETYPE GRAPH GENERATOR—Collects variables during real time data taking and prints out a graph at the end of a run.

65. MICRO-BASIC—BASIC Interpreter for the M6800.

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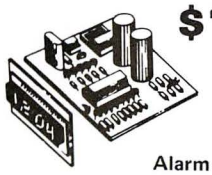

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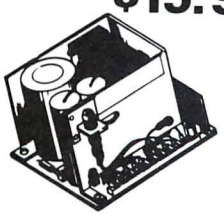

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Letters to the Editor

Dear Mr. Berkey,

My name is Michael Lillard and I am a 7th grade student at Hunter College High School in New York City. I have been assigned a Social Studies project concerning business and advertising. I decided to manufacture computers and advertise in trade magazines, such as yours. I would like to know how much your advertising rates are, so I can better manage my budget, and any other helpful information that you could send me.

Many Thanks,
Michael Lillard

Dear Michael:

Your letter was a pleasure to receive and I hope the following will help you with your worthy class project.

If I was to organize a new company for the purpose of manufacturing and selling microcomputers, here's how I would commence my promotional program.

1. Establish a rough budget ($20,000.00 to $50,000.00).
2. Assign a creative advertising agency to my account. (He'll work on a retainer fee basis, or standard 15%.)
3. Organize my collateral material (sales literature, brochures, etc.) with sales appeal on why my microcomputer has the best features. (estimated literature cost, $3,000.00.)
4. Write press releases of the features of my new microcomputer and send to all editors of recognized magazines and industrial computer publications.
5. Prepare advertising copy based on the *features* of your new microcomputer. Be specific about why you have the *very best* equipment on the market. The greatest *impact* for your initial display advertisement should be a main consideration. Consider a full page in color, or a two-page spread.
6. Select two of the magazines which you consider most important in reaching your potential customers.
7. Consider continuity for your advertising exposure. Plan at least a solid six month program (six consecutive issues of the two magazines you select). Prepare to analyze the effectiveness after the first four months, then set the next six months.
8. Establish a firm budget based on the above, and allow yourself an additional 25% contingent budget for special promotions. One of the major accomplishments for you to tackle right off the bat, Michael, is to become known as quickly as possible as a leading manufacturer in the microcomputing market. Advertising will help your company become known very quickly and, of course, help sell your new products.

From many years experience, Michael, I can tell you that there have been many very worthy products developed by innovative engineers and scientists who have attempted to start off their business with not enough marketing knowledge, and not enough operating capital, who have *failed* almost as quickly as they attempted to commence. Proper financial backing and marketing intelligence is the key to the success of most products (computers or otherwise) regardless of its dollar value to the consumer.

Enclosed is our rate card for INTERFACE AGE magazine so that you can prepare yourself a budget, based on the objectives you have outlined for your new company.

Please let me know if I can add more to your project. Why not send me a copy of your completed work after you've presented it to your teacher. Good luck and thank you for the opportunity to be of help.

Sincerely,
Bruce Berkey
National Sales Manager

Dear Editor:

I am interested in building a microcomputer system, but find it difficult to obtain *schematics* for the boards I want to build. (Z-80 CPU, 2102 memory, serial I/O port, TV TTY, cassette interface, etc.) Do you know of a source for this information? I would appreciate any help you can give me. Thank you.

Sincerely,
Graham M. Smith
Scotch Plains, N.J. 07076

Editor's reply
Most manufacturers will provide schematic if a stamped self-addressed envelope is provided. Z-80 CPU - Cromemco, TDL 2102 - Cromemco, Seals, IMSAI, ALTAIR Serial I/O port - Processor Technology Cassette Interface - Tarbell, IMSAI, Digital Group.

Dear Editor:

In the December issue of Interface Age there was an article written describing the Technico TEC 9900-SS 16 Bit Microprocessor Board. The article failed to include Technico's address and phone number. For anyone interested in further information on the Technico Board, please contact Technico, Incorporated, 9130 Red Branch Road, Columbia, Maryland 21045. Phone No. — Area Code 301 - 461-2200 or 1 - 800 - 638-2893.
Bill Regan
President - Technico, Inc.

Dear Editor:

I read your December issue cover to cover but felt I am getting enough material from my five other subscriptions. Then I picked up your March issue and it is just too good to pass up. Your Software Section is fantastic, here is my subscription, keep up the good work.
Adrien O. Miller
Brandon, SD 57005

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FOR SALE: Complete factory assembled Sphere system: 6800 MPU, keyboard, CRT, power supply, resident monitor in PROM, 4K user memory, 2 cassette I/O. Asking $1000.00 or willing to trade for a 924 Porsche. Bob Wada (714) 893-8940

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FOR SALE: Imsai 1-UCRI cassette board $39.00, 1-8080 processor board $160.00, 1-4 port parallel I/O board $140.00, 1-2 port serial I/O board $140, 2-parallel board cables $20.00 ea, 2-serial board cables $15.00 ea., 1-SWTP PR-40 printer $240.00, 1-Oliver Audio paper tape reader $60.00, 1-DC-50 MHz RF generator $200.00, 1-Motorola PT-300 handi talkie $250.00, Software by Scelbi, 1-Scelbal higher level lang. $35.00, 1-8080 assembler $20.00. All boards fully assembled and guaranteed to work. Will shop COD UPS you pay the freight. Vance James, P.O. Box 2292, Hickory, N.C. 28601.

CRT TERMINAL. 3-month old Micro-Term ACT-1 with 9" Sanyo monitor for sale. 16 lines of 64 chars, auto-scroll, 110-300-600-1200-2400-4800-9600 baud, RS-232C or current-loop. Modified for direct display of typed data. All documentation. $495 includes shipping. Bob Ripley, Route 3, Fayetteville, AR 72701. (501) 267-3172 evenings.

CARD READER with documentation $100.00 + shipping cost or trade. Bob Stevens, 2361 E. Foothill Blvd., Pasadena, CA 91107. (213) 449-0616.

IMSAI I-8080 kit — never assembled. Has 22 slot mother board, $490. PIO4-1, $10;PIOMs, $16.50; SIO2-2, $119; RAM 4A-4, $105. Send SASE for info. First checks will take the gear. Include shipping costs; excess will be refunded, or arrange local pickup. S.R. Lewis, 1477 Barrington, #17, L.A. CA 90025.

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SELL YOUR PRODUCTS IN FRANCE. American with a new French company wishes to represent U.S. products which have not as yet been exploited in Europe. If you feel your products are exportable — write to me with full details P. Studner, SUPER SEARCH, 39 Avenue de Breteuil, Paris 75007, France.

FOR SALE: Altair 8800, working, hardly used, ICs in sockets, flat-cable to front-panel, $440 or offer. BYTE Shop TV typewriter, new, working, $110 or offer. Dennis Feucht, 2015 S.E. 51st Ave., Portland, OR 97215. (503) 233-2648 or (503) 644-0161 ext. 6255.

—WANTED: MITS ALTAIR disc (88-DCDD) with disc basic. Need not be in working condition, but must be complete. State age, condition, version basic, price and other particulars. Dana G. Peterson, 2129 Harper Street, Lawrence, KS 66044; (913) 841-2817.

PDP-8 MINI COMPUTER (Straight-8) for sale or trade. Mounted in attractive walnut cabinet (wife approved for den). Complete with maintenance manual, drawings, 4K Basic, 4K Focal, Editor, PAL III assembler, Disassembler, TTY interface, games, etc., etc. Perfect condition. Free DECUS membership available for additional software. Presently in use with ASR Model 33 teletype. Can be sold with or without teletype. Sale price w/o teletype $800.00. Rex Eagle, P.O. Box 10498, Charlotte, N.C. 28288. (704) 374-6557.

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The authors in this issue would like to know your feelings as to which article you consider the best. You may cast your vote on each article or only one, which you prefer. The articles are graded on point scale 1 (lowest) to 10 (highest). At the end of the voting period all votes will be tallied and the highest scoring article will be announced and the author will receive $100 bonus.

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8. EXMON — 6800 Extended Monitor System
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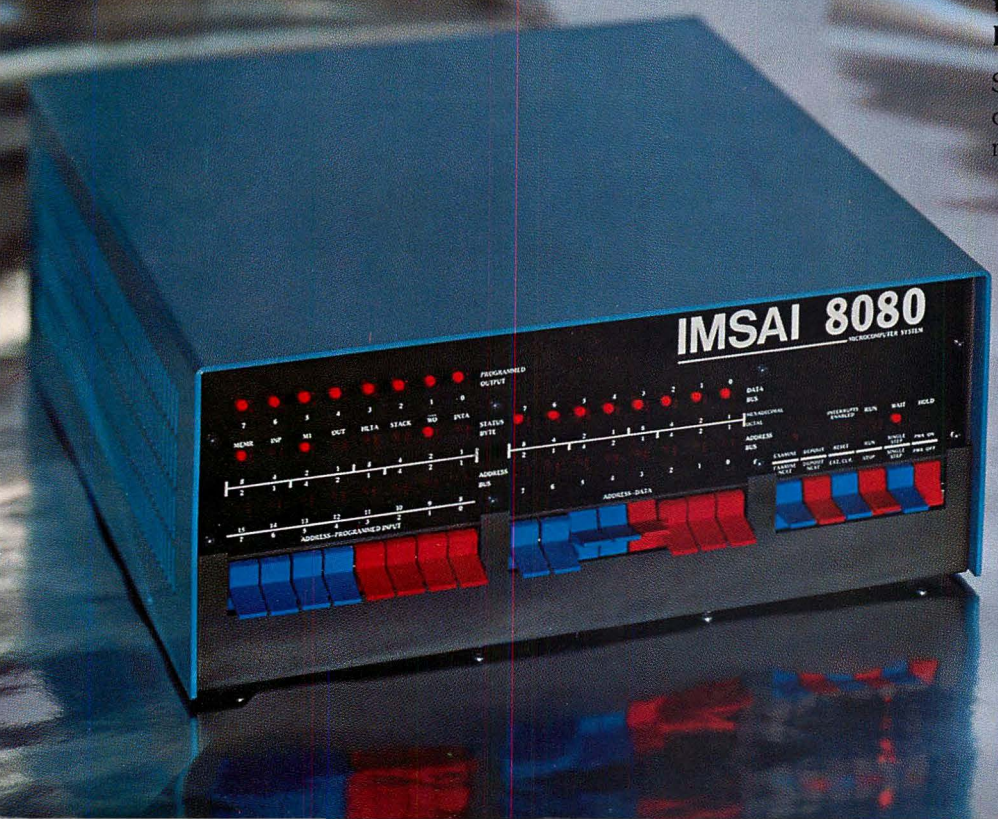

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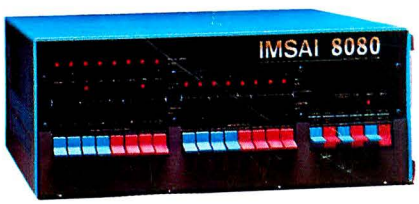

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